

Model Name: GA-Z68XP-UD3-iSSD

SHEET

TITLE

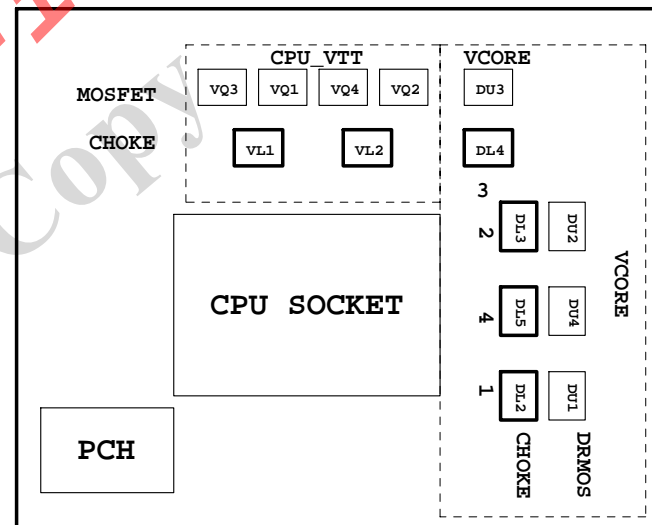
1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PI7C9X113SL
19	PI7C9X113SL POWER
20	PCI SLOT 1&2
21	I/O ITE8728
22	COM, -PROHOT, ESATA CONNECT
23	Dual BIOS , TPM SLB9635TT
24	ALC892
25	REAR AUDIO JACK
26	VCORE PWM_ISL6366CRZ-1
27	VCORE PWM_ISL6366CRZ-2

28	VCORE PWM_ISL6366CRZ-3
29	DISCRETE POWER I
30	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ
31	CPU_VTT PWM_ISL6322G
32	VCCSA POWER
33	F_PANEL , F_USB , FDD
34	ATX POWER, CLOCK GEN
35	HWM,KB/MS , FAN CTRL
36	REALTEK RTL8111E
37	ESATA SE9128
38	FRONT NEC USB3.0
39	REAR NEC USB3.0
40	TABLE LIST



Component value change history

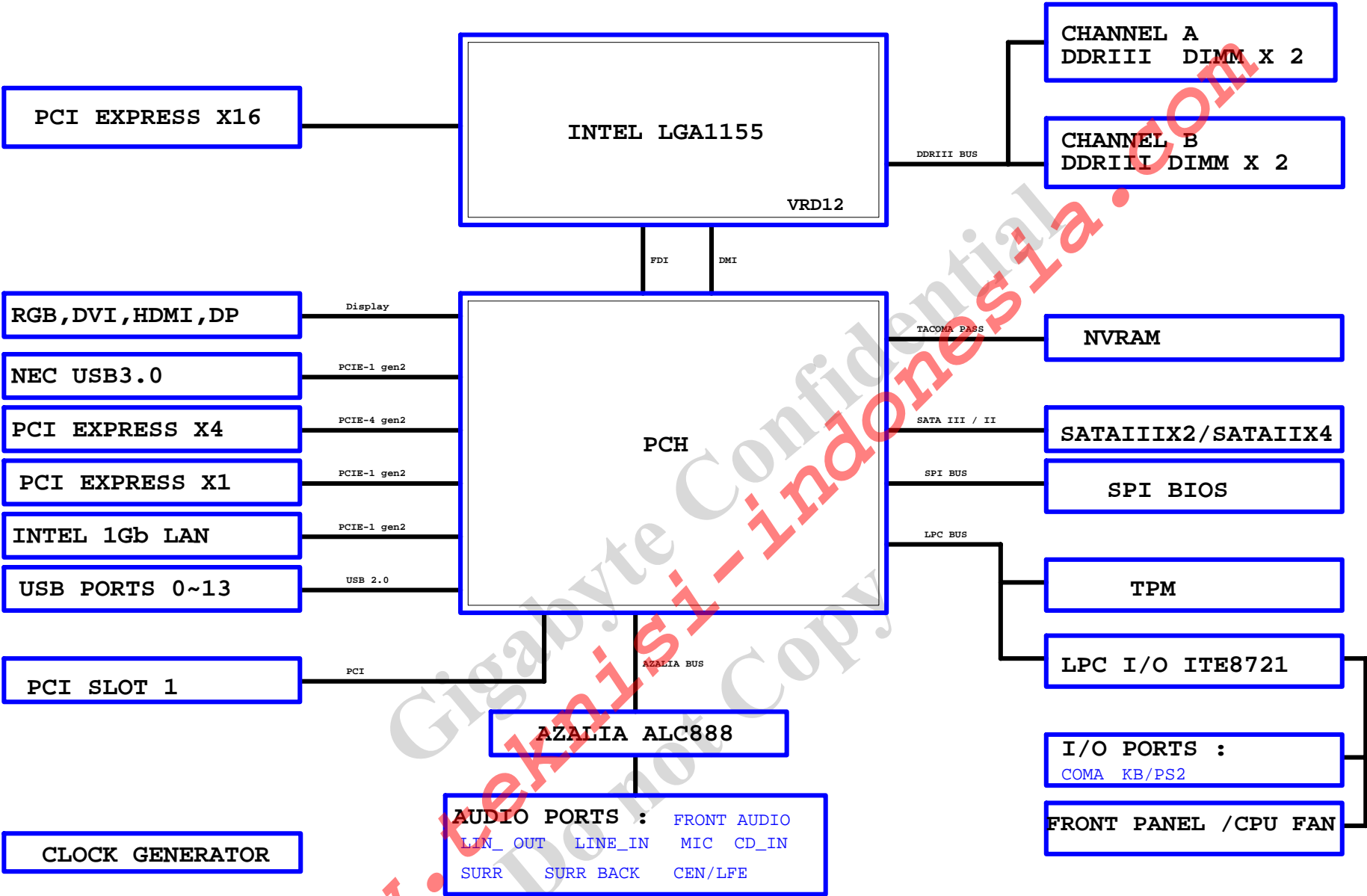
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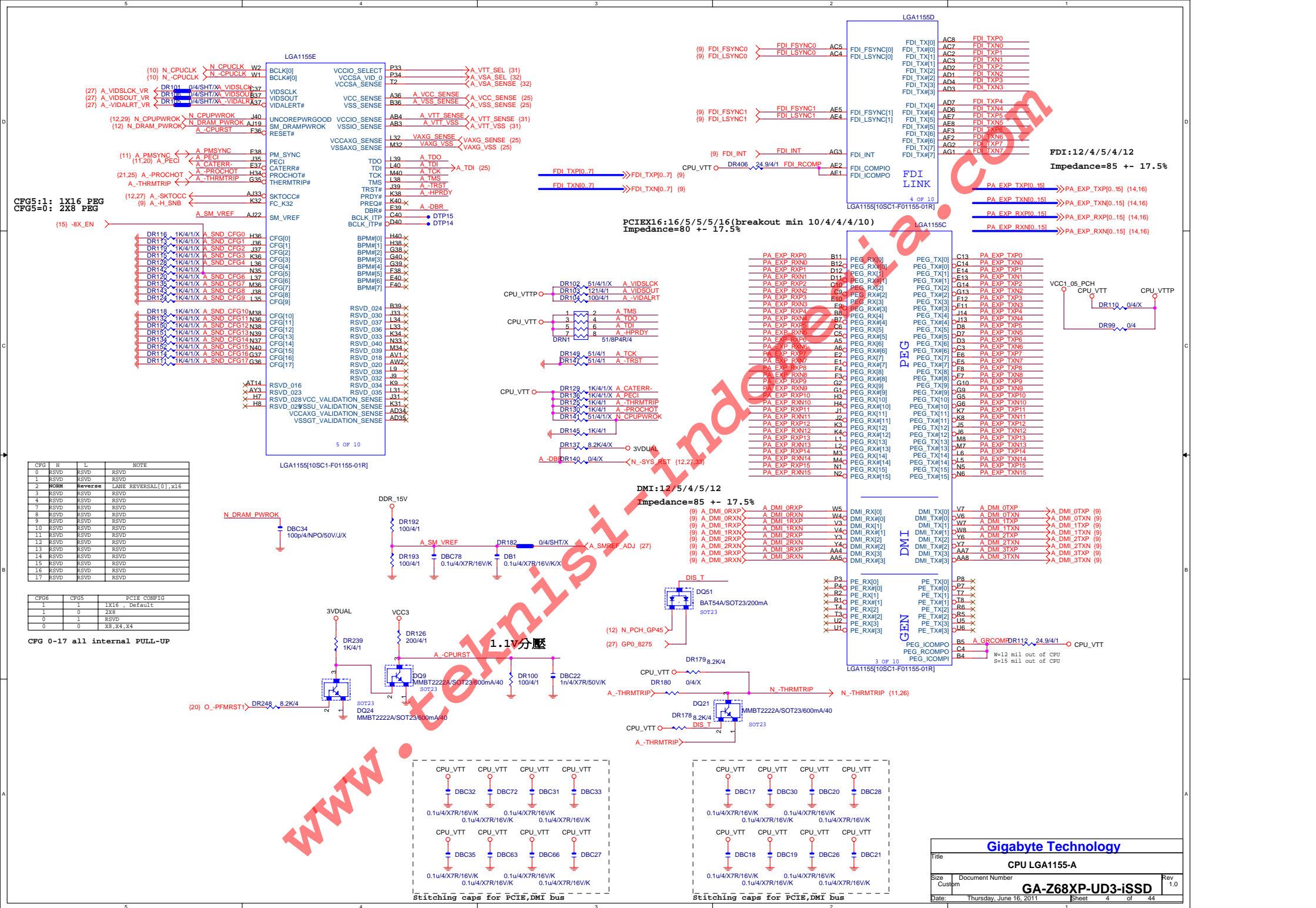
DATE	Change Item	Reason
P67X-UD3-B3 REV0.1	1. EVT Release	
	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11 2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
P67X-UD3-B3 1.0-0308	1. Add "Dolby" logo	
1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68X-UD3-B3 1.02	1. 文字面 : P67X-UD3-B3 --> Z68X-UD3-B3	
Z68X-UD3-B3-new 0.1	1. Add M-SATA , HDMI , GPU 2. Remove usb3 turbo 3. M-SATA SWITCH的預留電阻type,注意走線	
Z68X-UD3-B3-new 1.0	1. 文字面 : Dolby change to DTS logo 2. 文字面 : SLOT部分全對齊 3. update MINI_PCIE footprint	

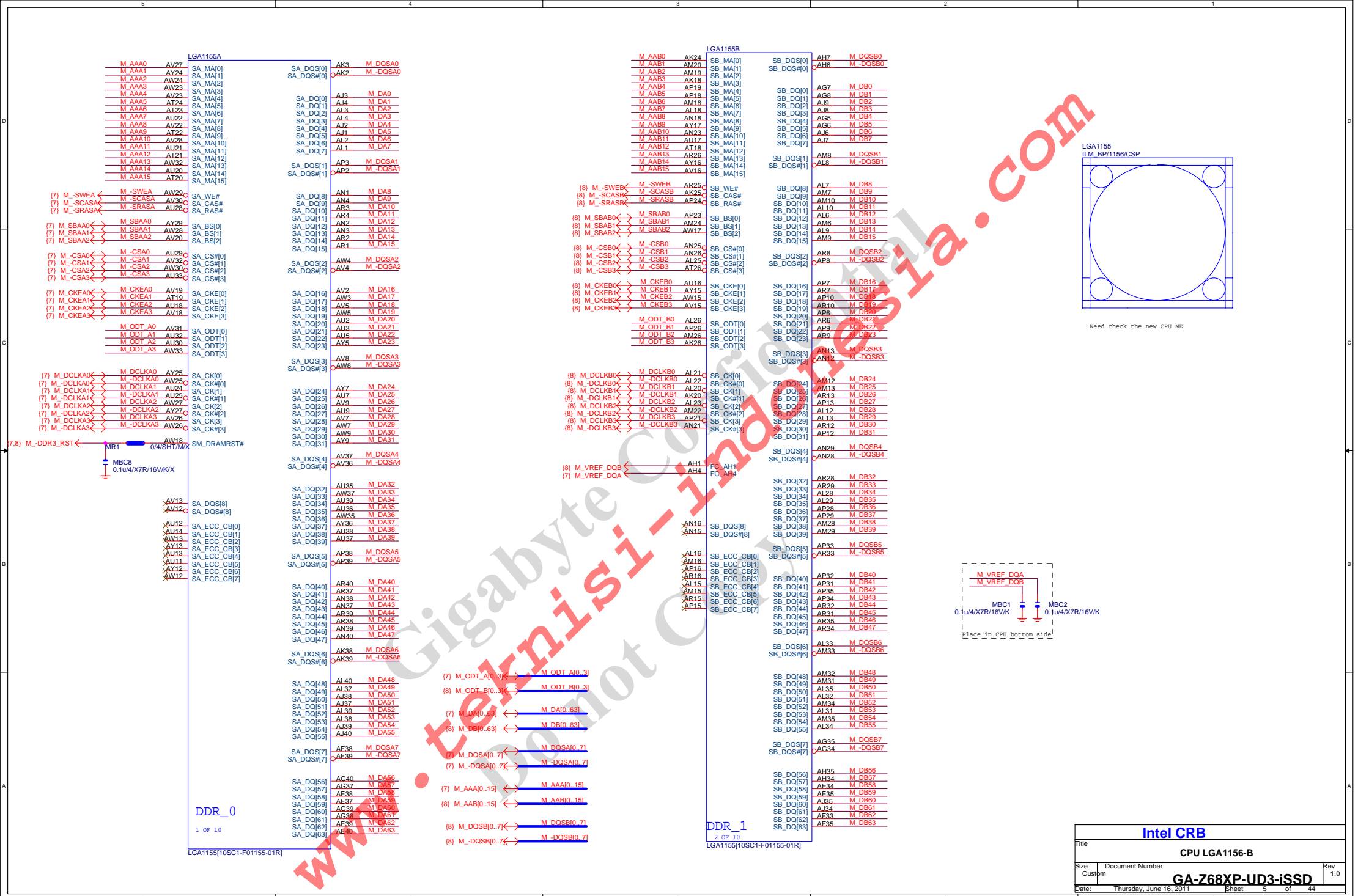
4. Add TM & TMS 0 ohm

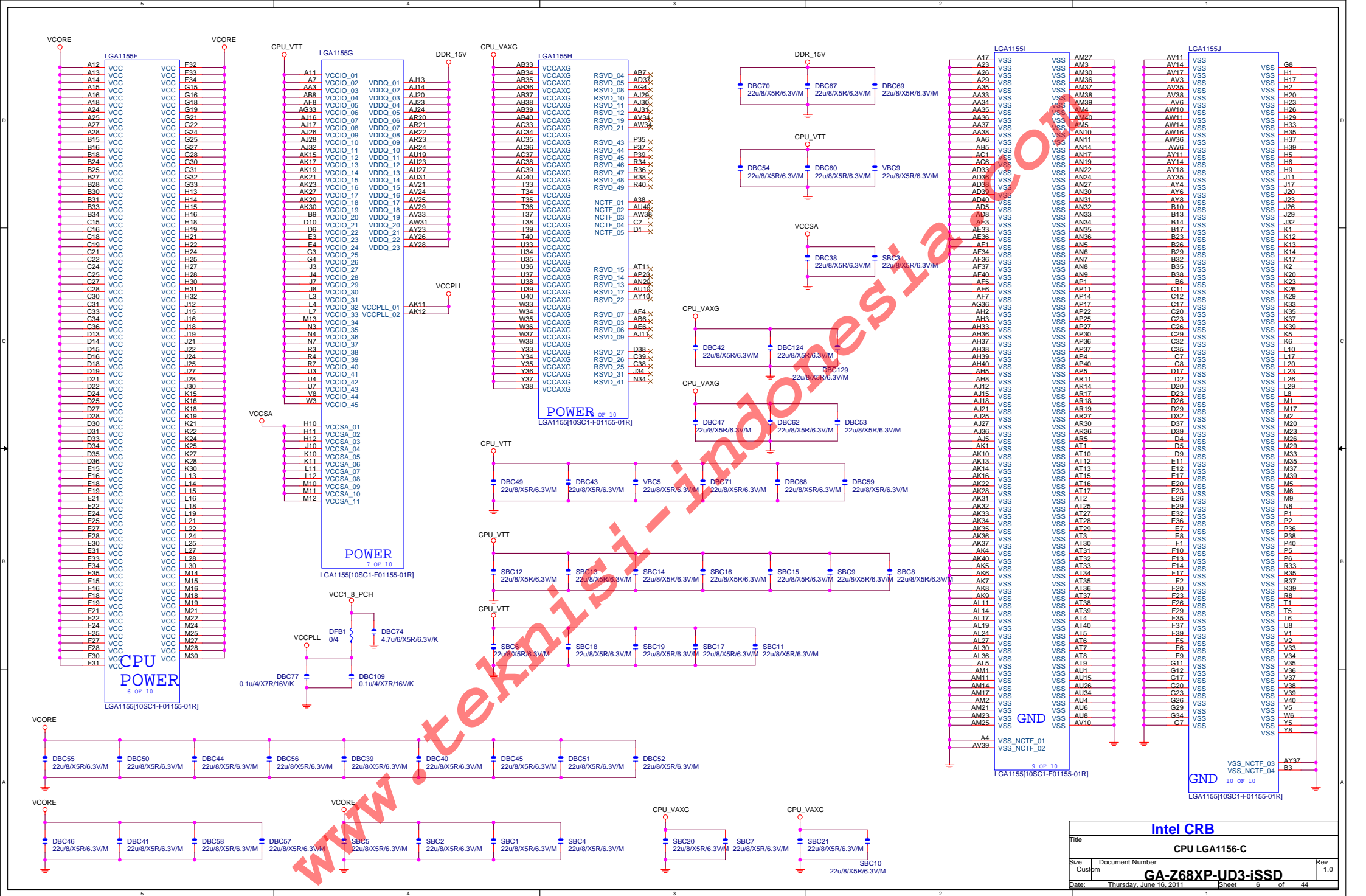
5. ITE8275_CLK CHANGE TO PCH.AW5

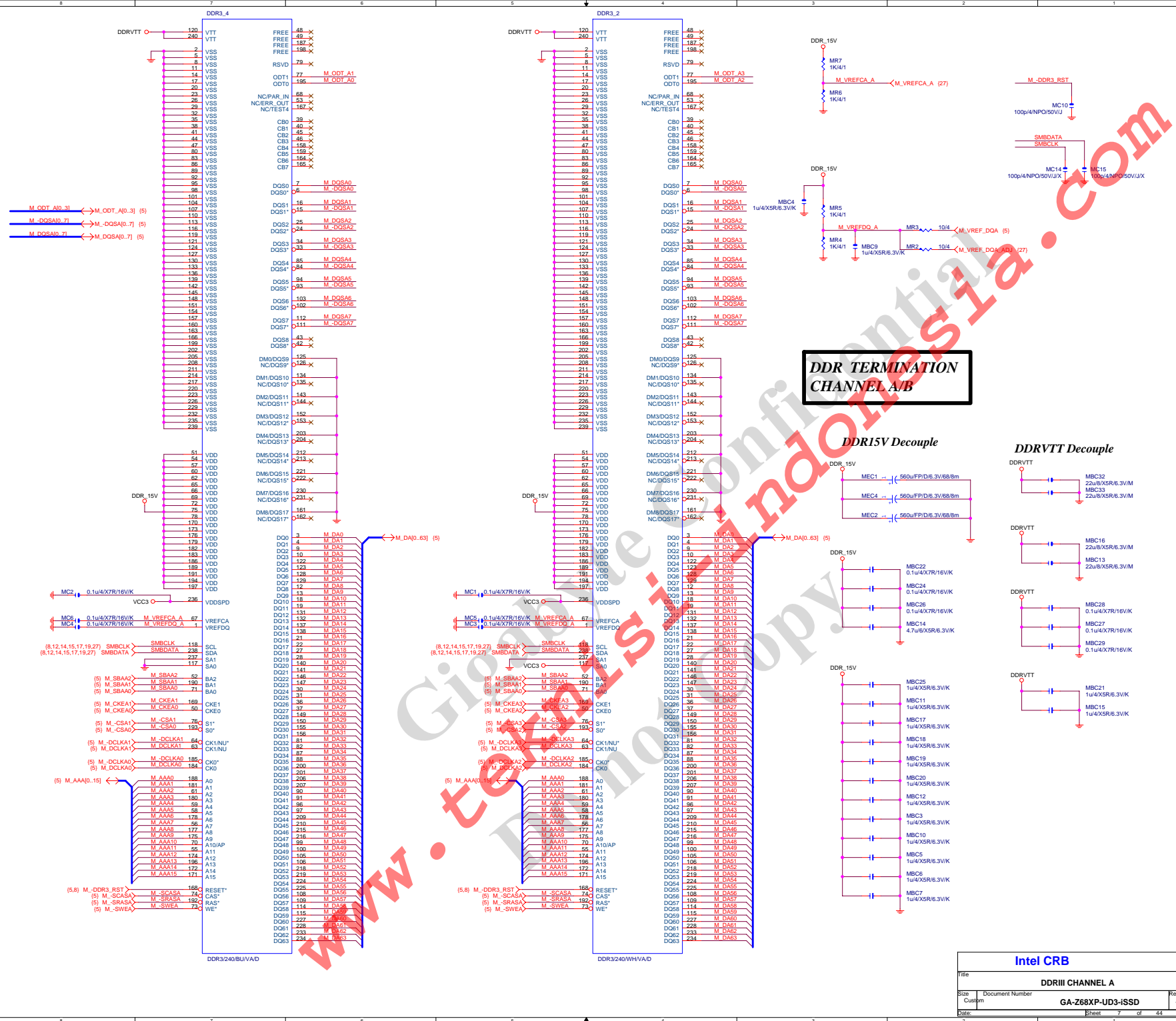
BLOCK DIAGRAM

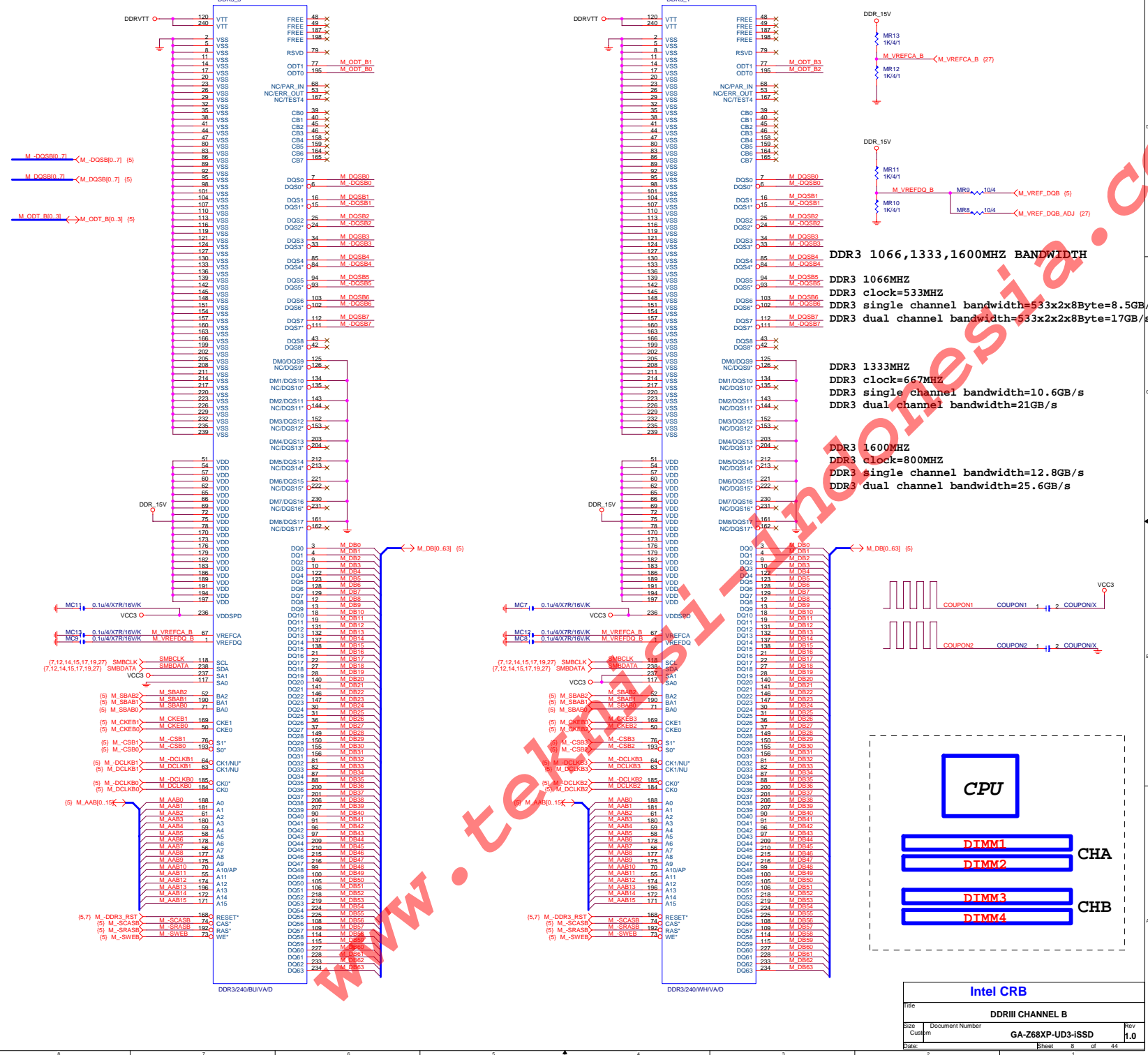




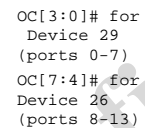








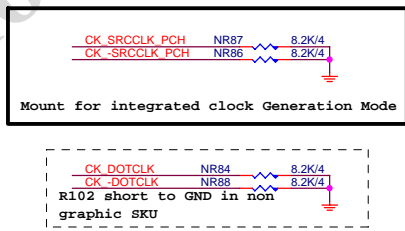
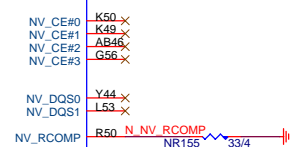
PCHG

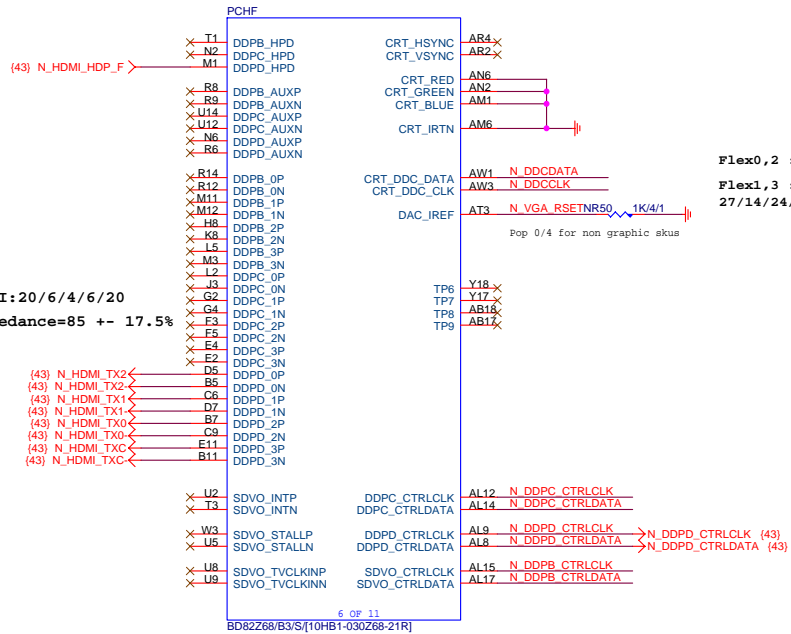


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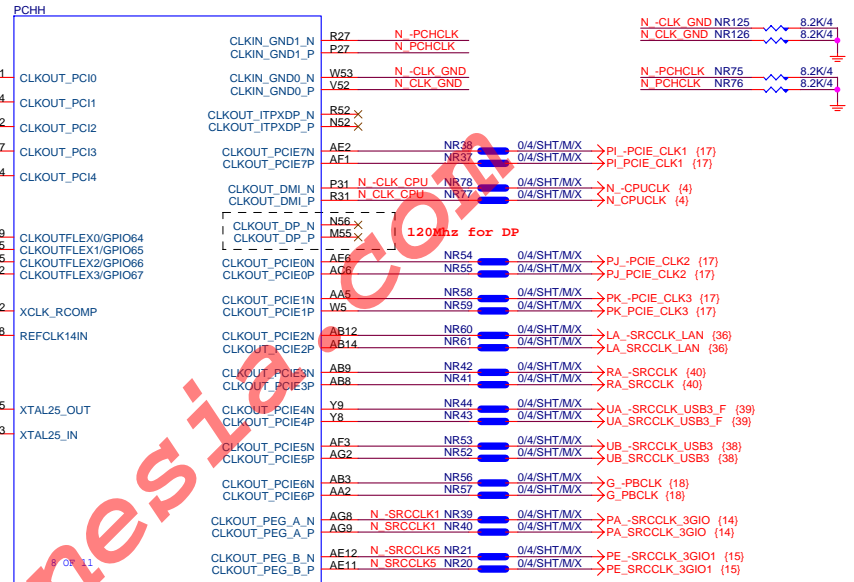
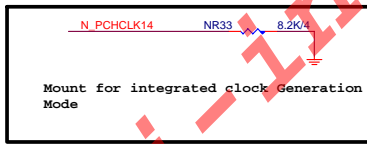
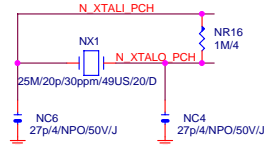
FDI TXP[0..7] >> FDI_TXP[0..7] {4}

FDI TXN[0..7] >> FDI_TXN[0..7] {4}





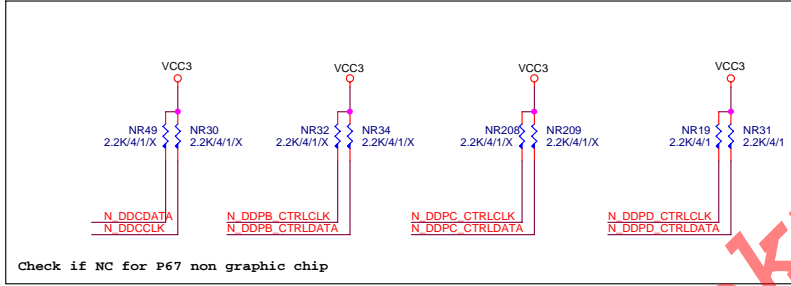
Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ



Differential Clock:18/6/4/6/18
Impedance=90 +- 15%

Pin	Type	Recommendations	Reason/Impact
INT13_V3V#	I/O	Default Mode: Internal weak pull-down. No Reset Mode with TCO Disabled: Connect to Vcc1_3 with 5.0k Ohm weak pull-up resistor.	
INT13_V3V#	I/O	Default Mode: Internal pull-up. Top Block Sleep Mode: Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/SP101B, GNT1#	I/O	Default (NFI): Lark built SATA1GP/SP101B and GNT1# floating. No pull-up required. Reset from PCI: Connect SATA1GP/SP101B to ground with 1k Ohm pull-down resistor. Leave GNT1# floating. Reset from LPC: Connect both SATA1GP/SP101B and GNT1# to ground with 1k Ohm pull-down resistor.	If LFC is selected BIOS may not be placed on LPC. Not all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid decoder in order to boot. Resetting to PCI is intended for debug/testing only. Boot BIOS destination (direct to LPC/PCI) by functional design or via Boot BIOS destination bit will not affect SPI accesses initiated by Management Engine or Integrated MMIO I/Os.
SATA2P/SP103B	I/O	Do not pull low.	BIOS chip for server platform. ONLY
HDA_SDD	I/O	Default: Do not pull high. Disable HEC in Manufacturing Mode: Connect to Vcc1_05_PCH with 1k Ohm pull-up resistor through a jumper.	Flash Descriptor Override
SPI_M0N0	I/O	Internal weak pull down. Do not pull high.	EMI R/F Termination Voltage
SPI_TVS	I/O	Internal weak pull up. Do not pull low.	EMI termination voltage
HDA_STM0	I/O	Internal weak pull down. Do not pull up.	On die P1_0k voltage selector
SP101B	I/O	Enable T1S: Pull up with 1k Ohm to Vcc1_05_PCH. Default (Disable T1S): Leave NC. Internal pull down.	Tx3 confidentiality
SP103B	I/O	RTN: Leave floating. Do not pull low. FECN: Pull low with 1k Ohm to ground.	PCIE: Can be override by softpin through ME.
SP102B	I/O	Internal weak pull up. Do not pull low.	On die P1_0k voltage regulator
SATA2GP/SP103B	I/O	Internal weak pull down. Do not pull high.	
SATA3GP/SP103F	I/O	Internal weak pull down. Do not pull high.	

GP29 , 35 , 36 , 37 power on with 3.3V pluse
GP8 always Hi without PU
GP20 with pluse during power on & reset

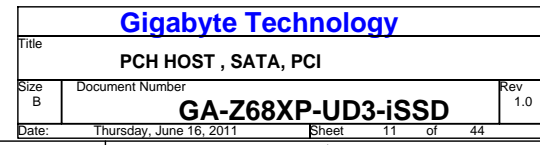


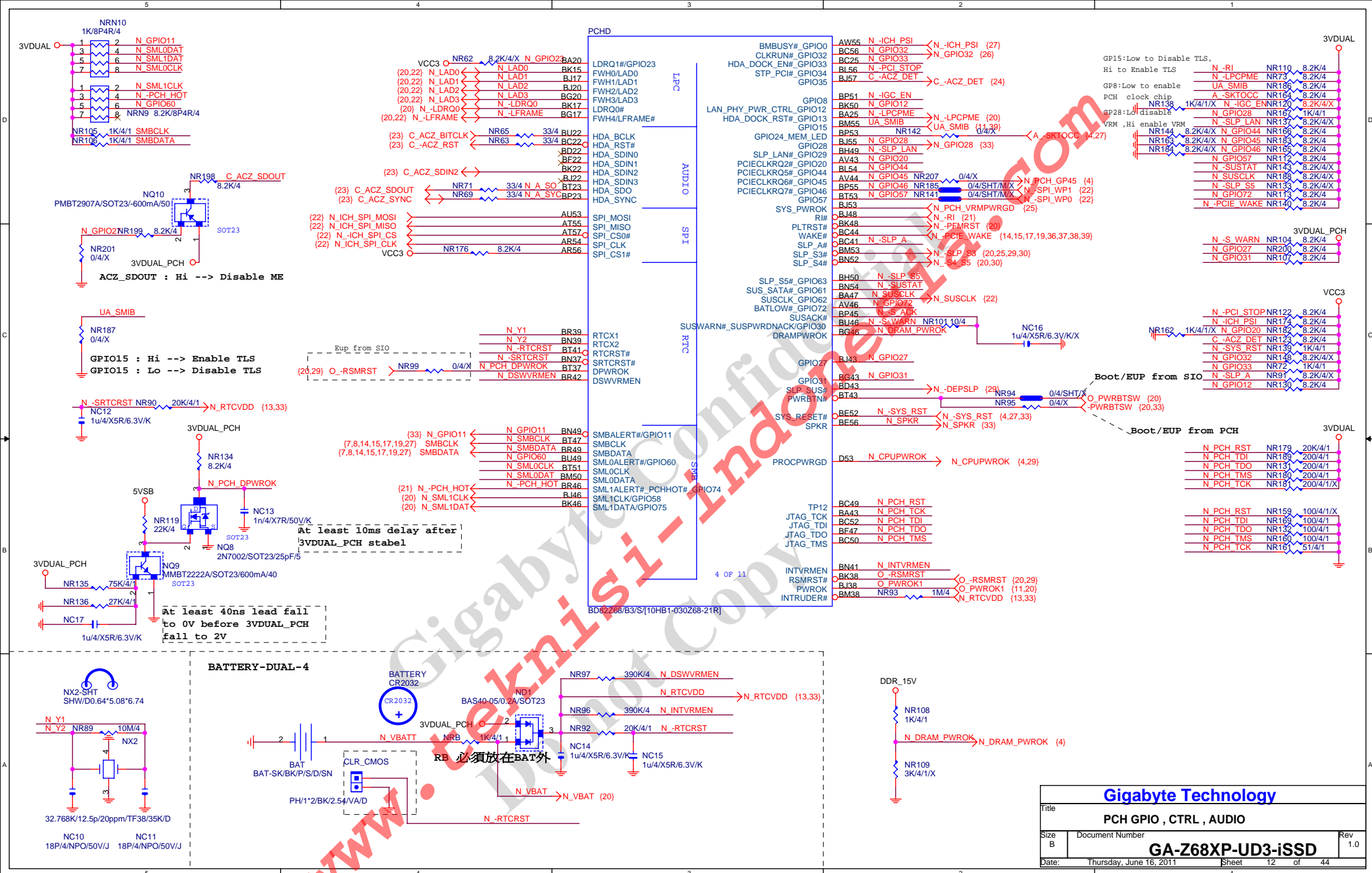
Check if NC for P67 non graphic chip

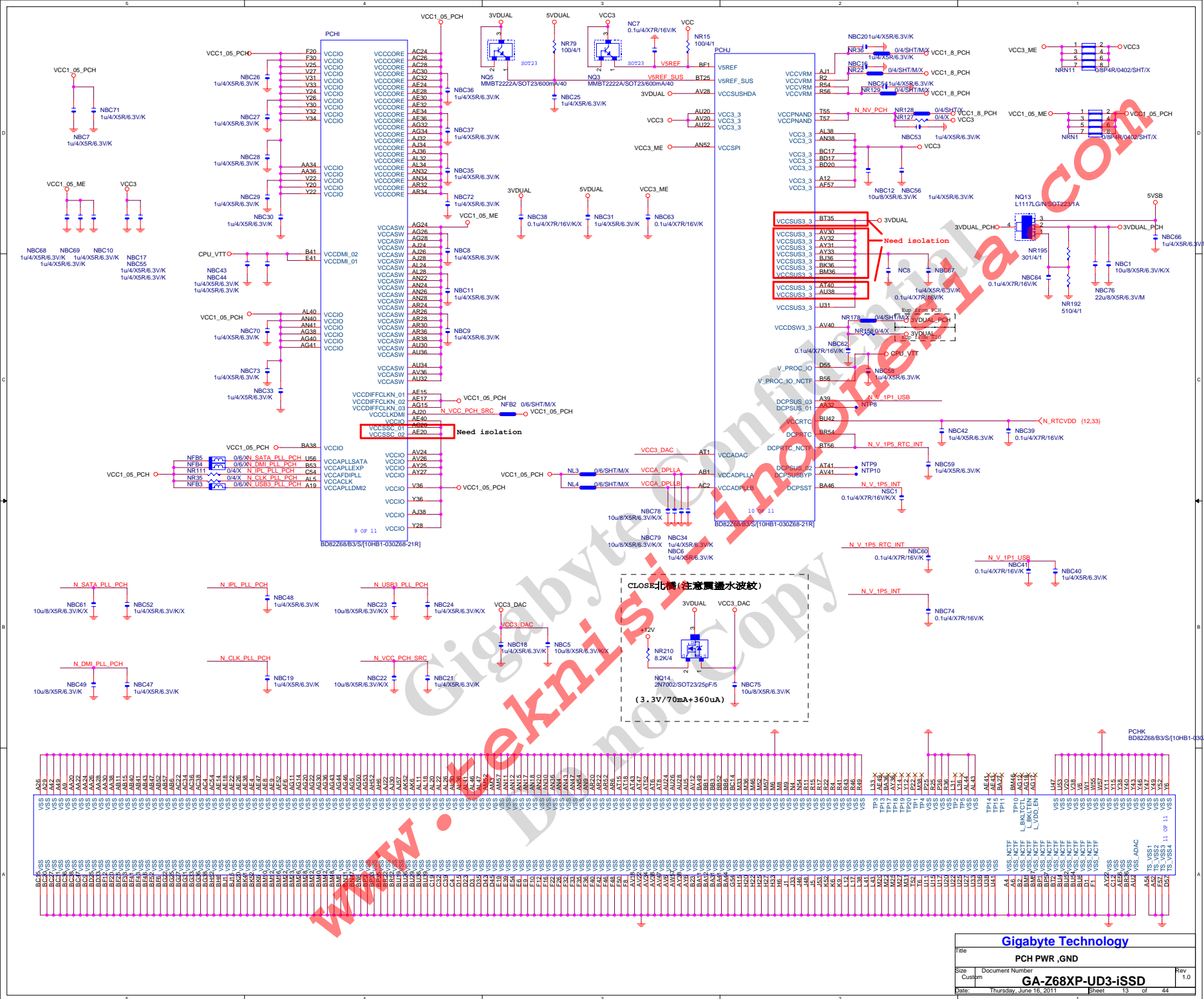
MB-ID

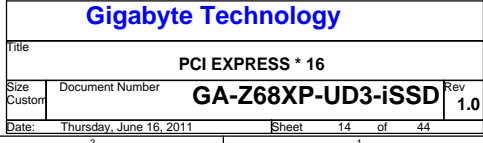
NR64 8.2K/4/X N GPIO17

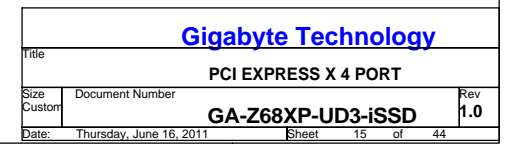
NR173 8.2K/4/X N GPIO19

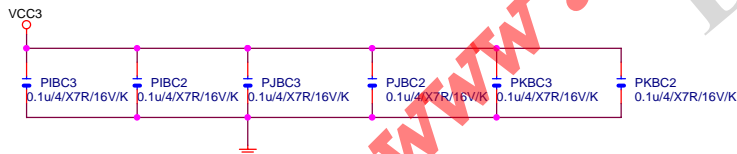
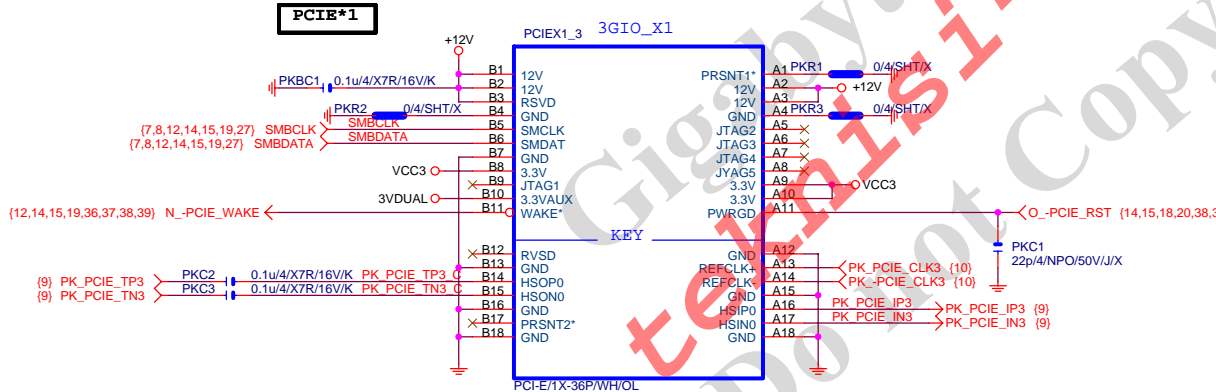
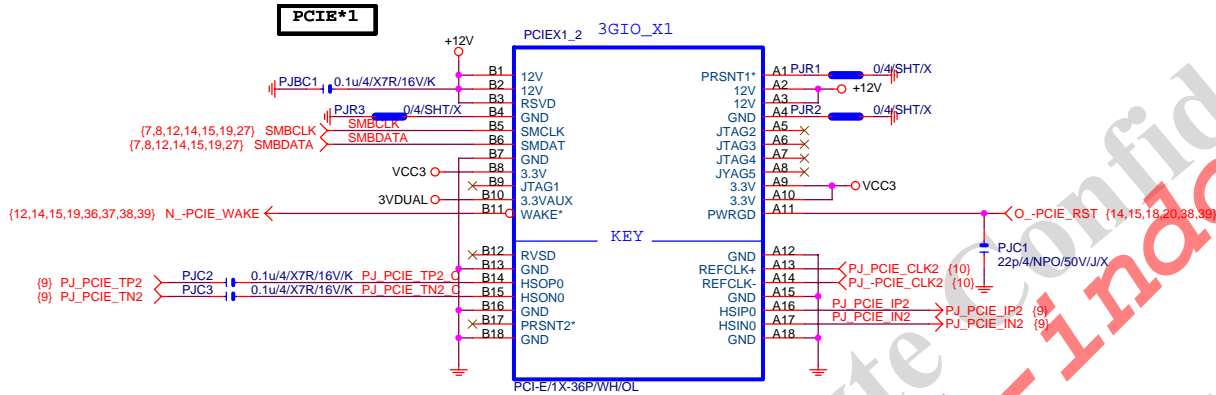
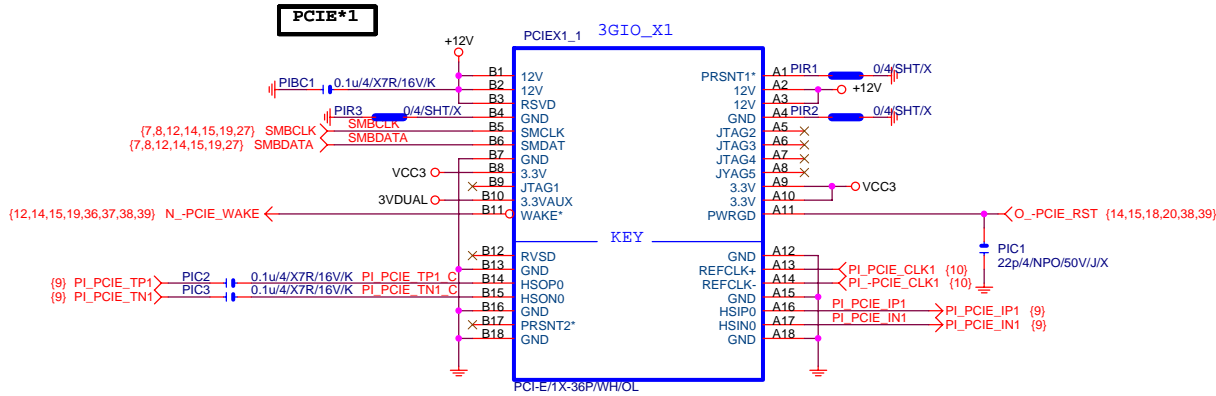




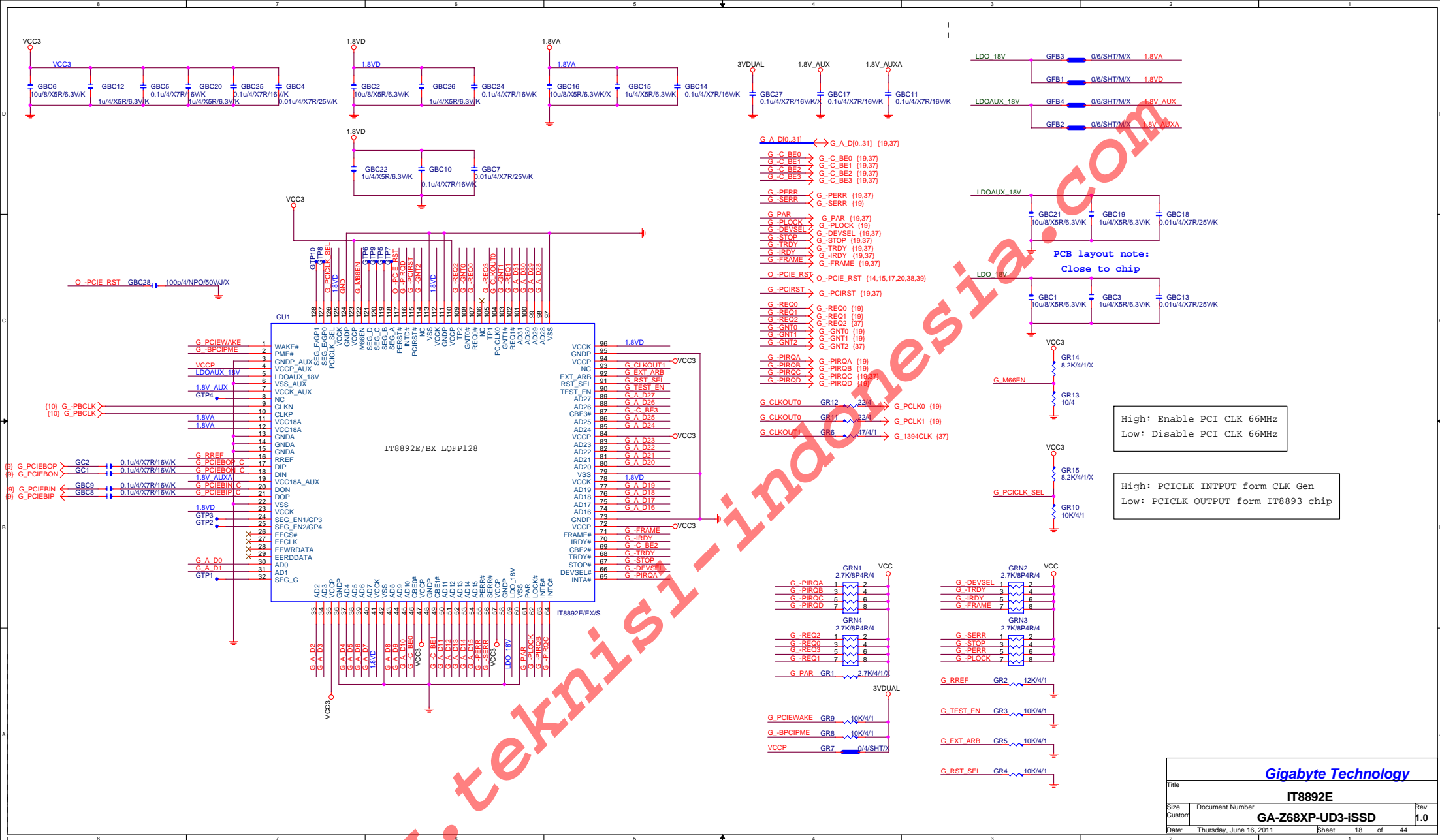


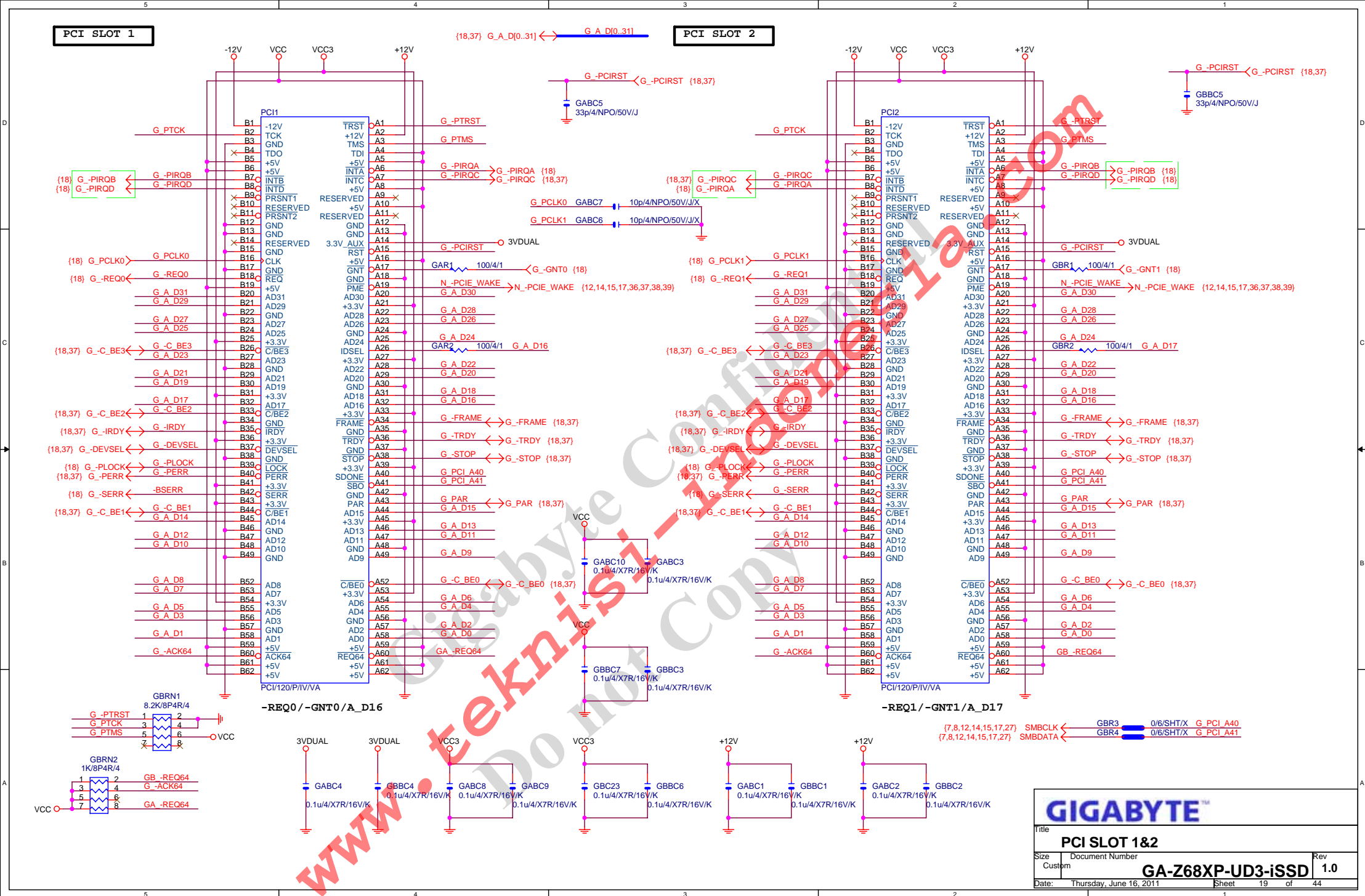


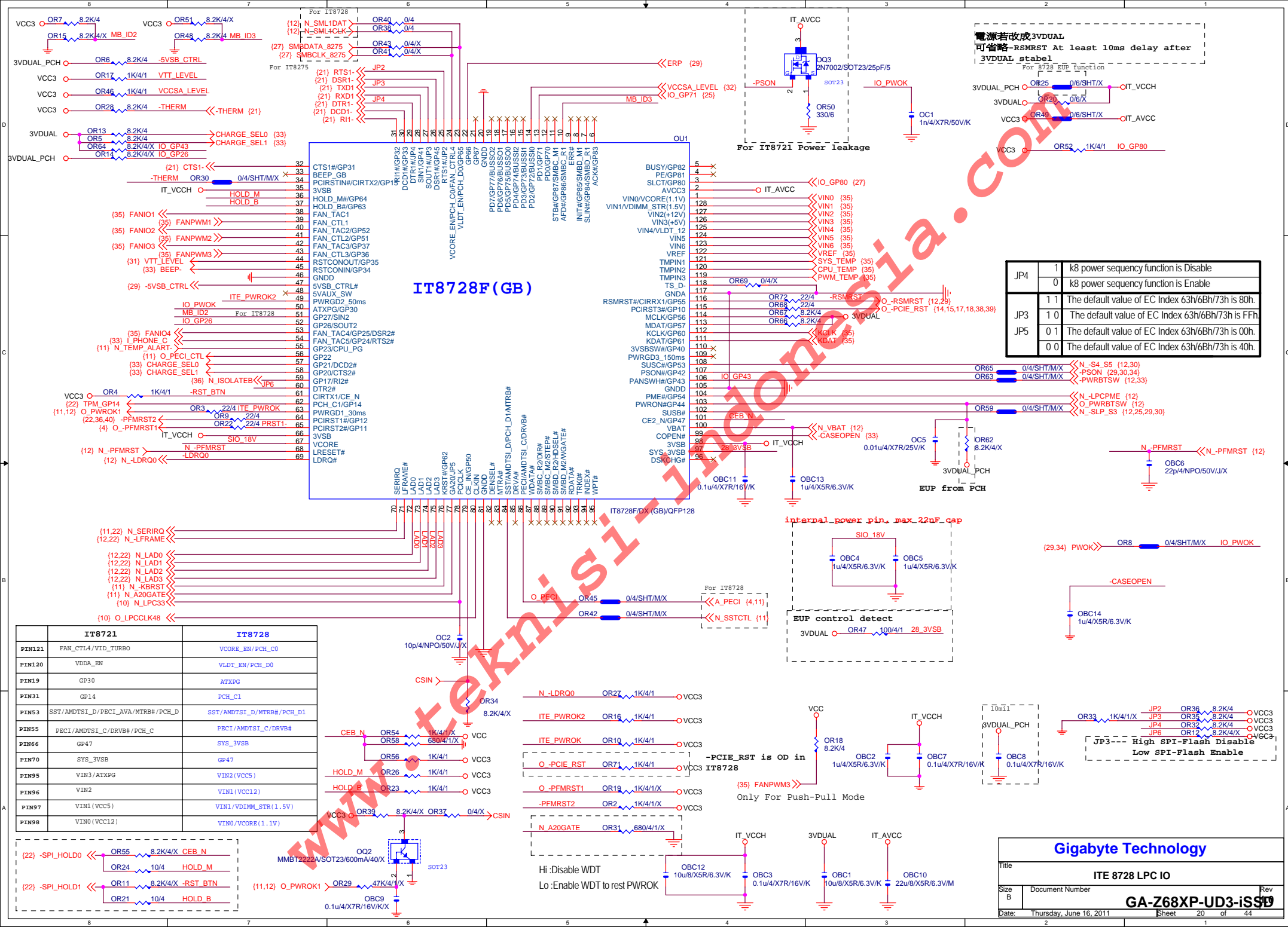




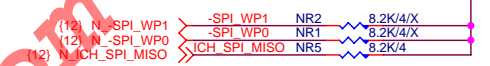
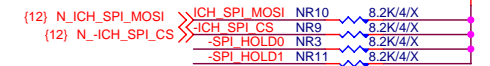
Gigabyte Technology			
Title			
PCIE_X1 1,2			
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MOSI For DMI RX Termination Voltage



Default int pull up



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

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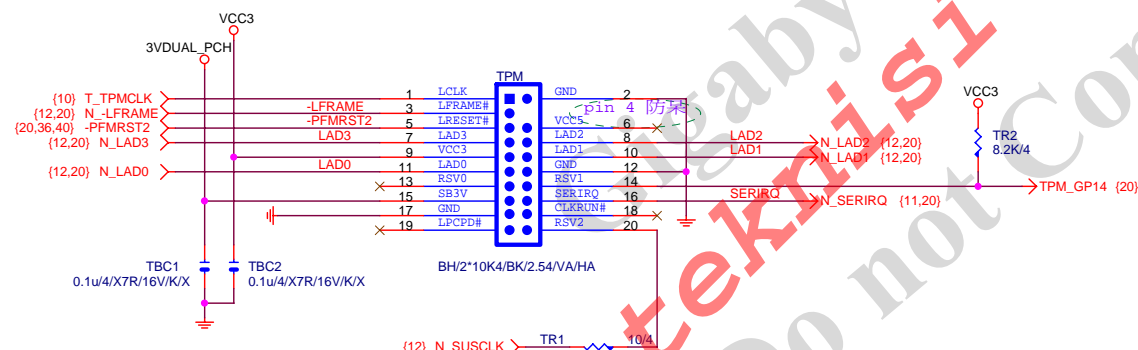
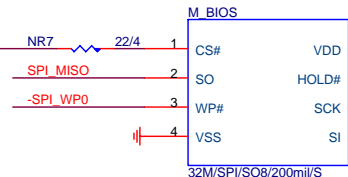
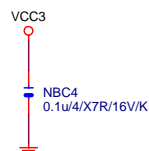


Diagram illustrating the connection of jumpers (JD) to resistors (CR) in the Digital Area and Analog Area.

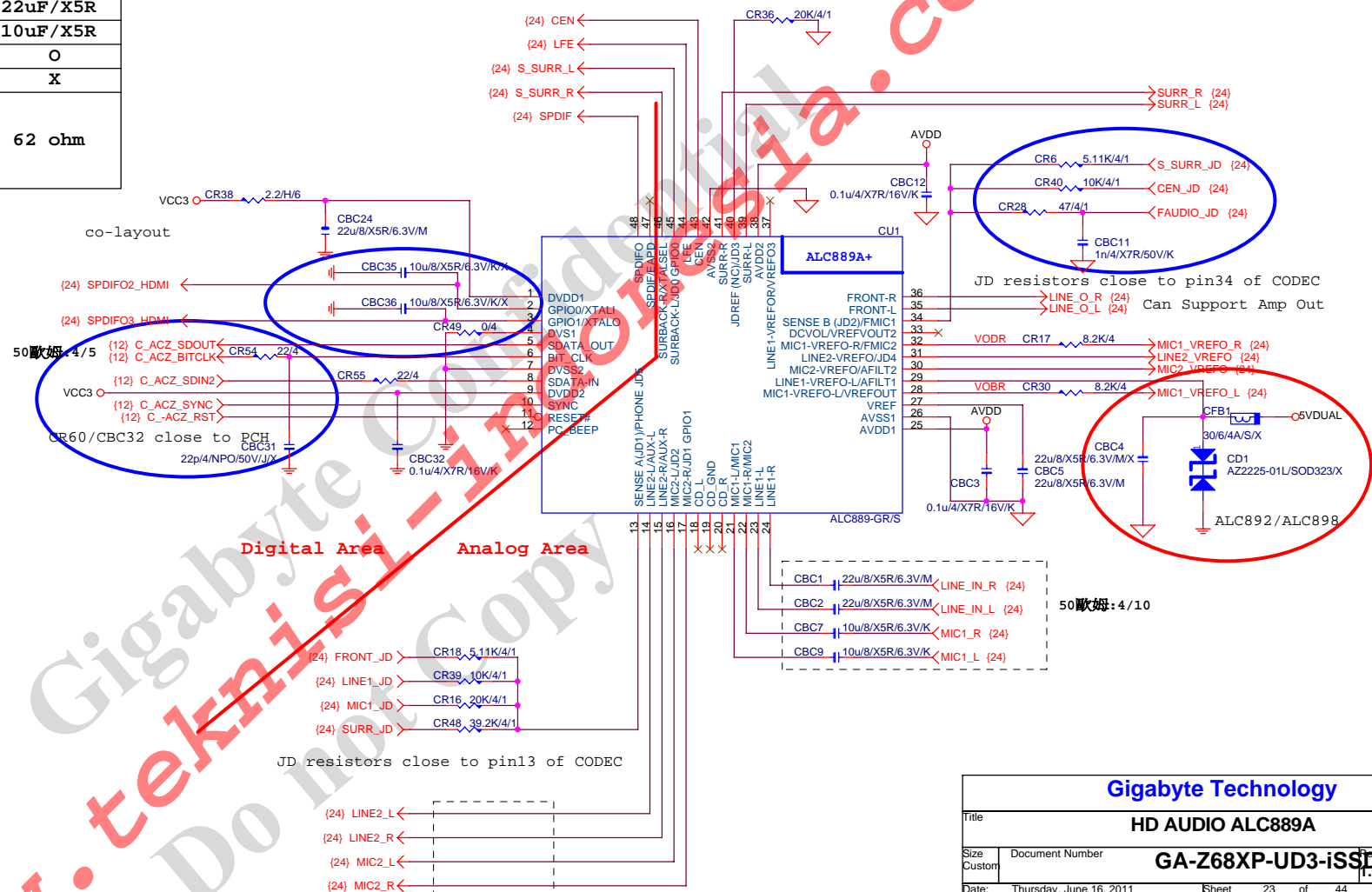
Digital Area:

- (24) FRONT_JD > CR18 5.11K/4/1
- (24) LINE1_JD > CR39 10K/4/1
- (24) MIC1_JD > CR16 20K/4/1
- (24) SURR_JD > CR48 39.2K/4/1

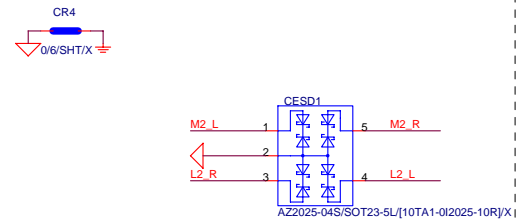
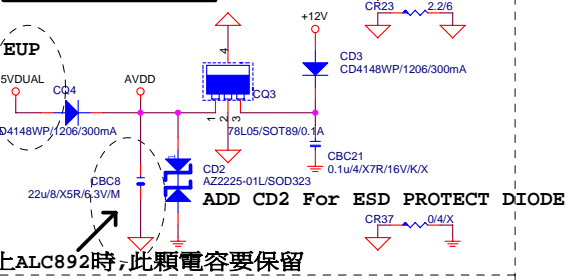
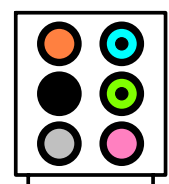
Analog Area:

- (24) LINE2_L < []
- (24) LINE2_R < []
- (24) MIC2_L < []
- (24) MIC2_R < []

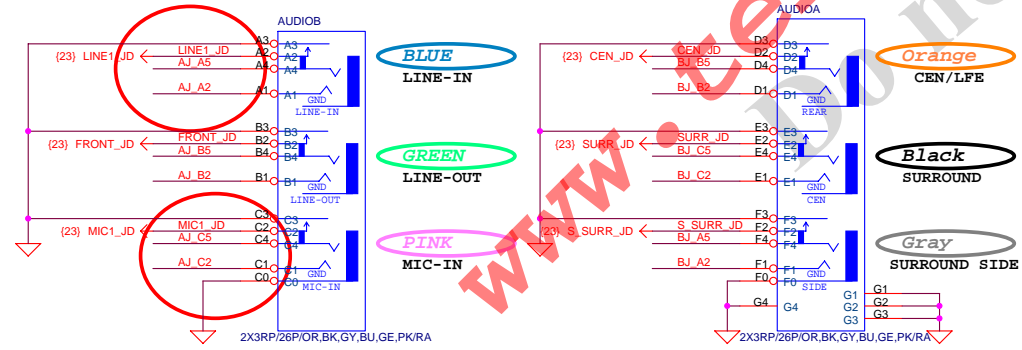
JD resistors close to pin13 of CODE



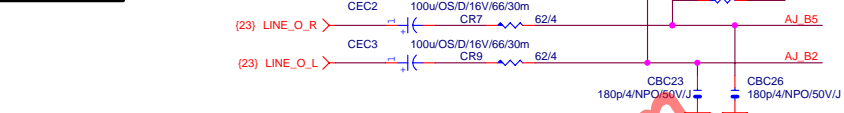
CODEC POWER/EMI PAD

AZALIA JACK
BTX AZALIA CONNECTOR

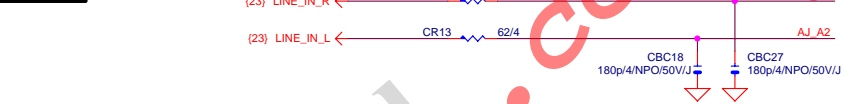
11NR6-403007-21R



LINE-OUT



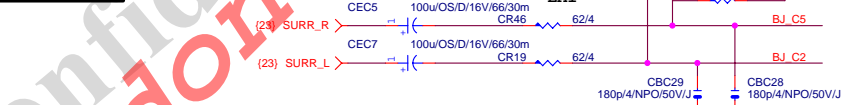
LINE-IN



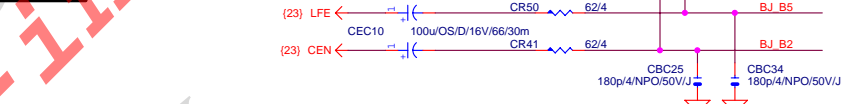
MIC-IN



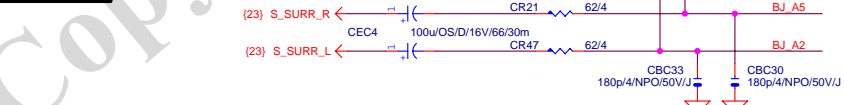
SURROUND



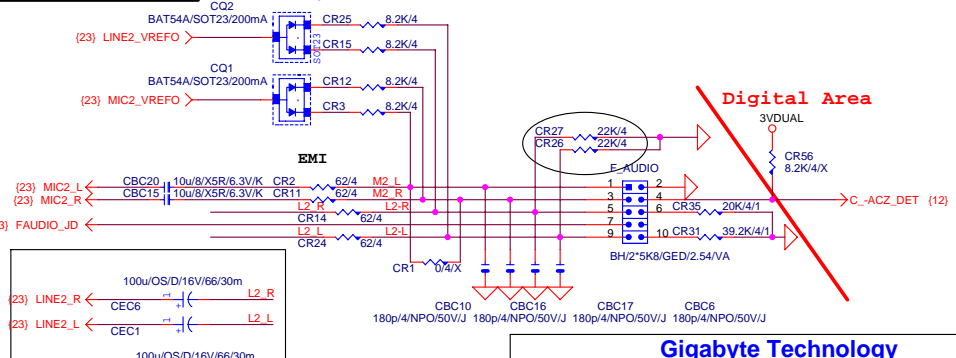
CEN/LFE



SURR BACK

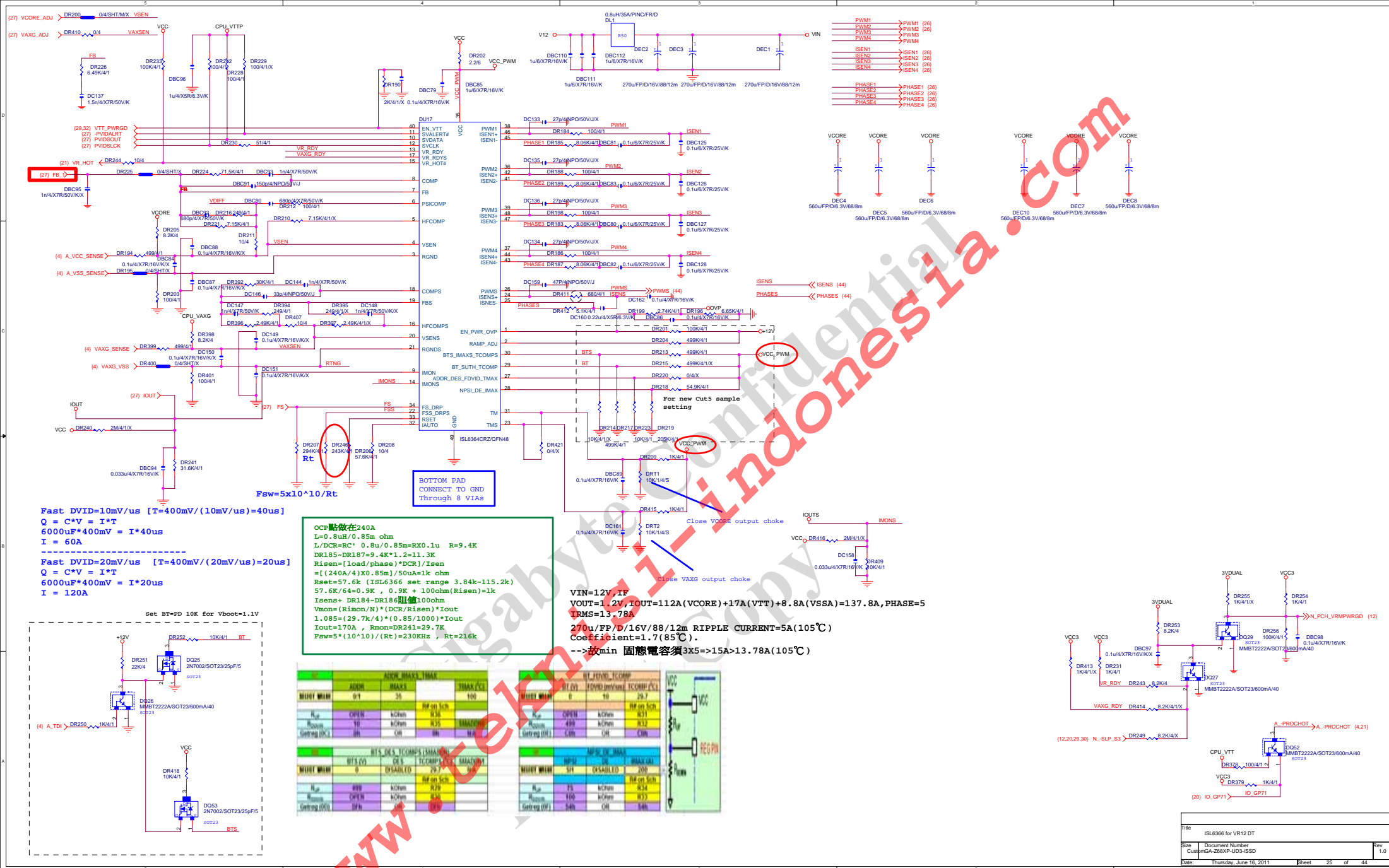


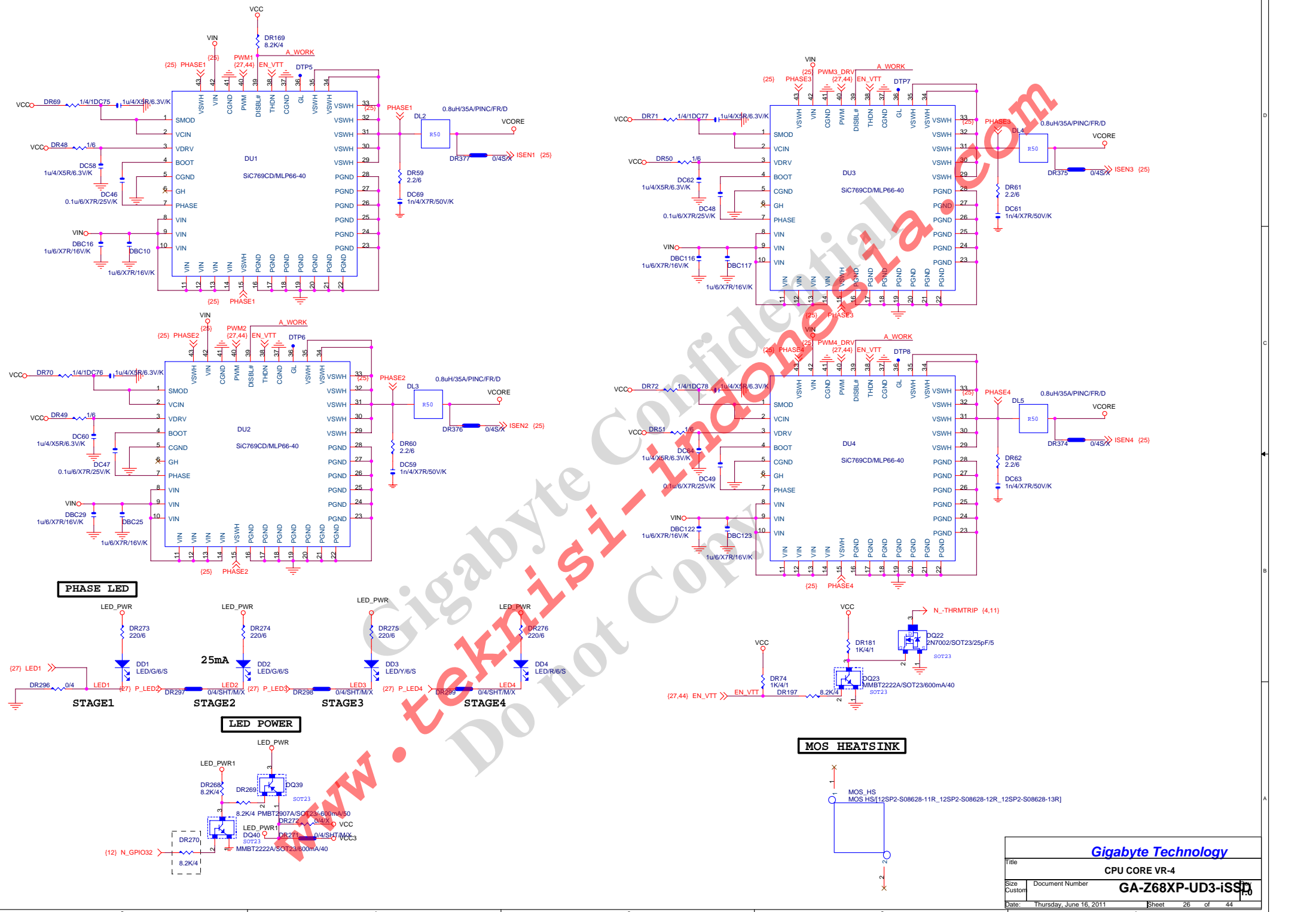
AZALIA FRONT PANEL

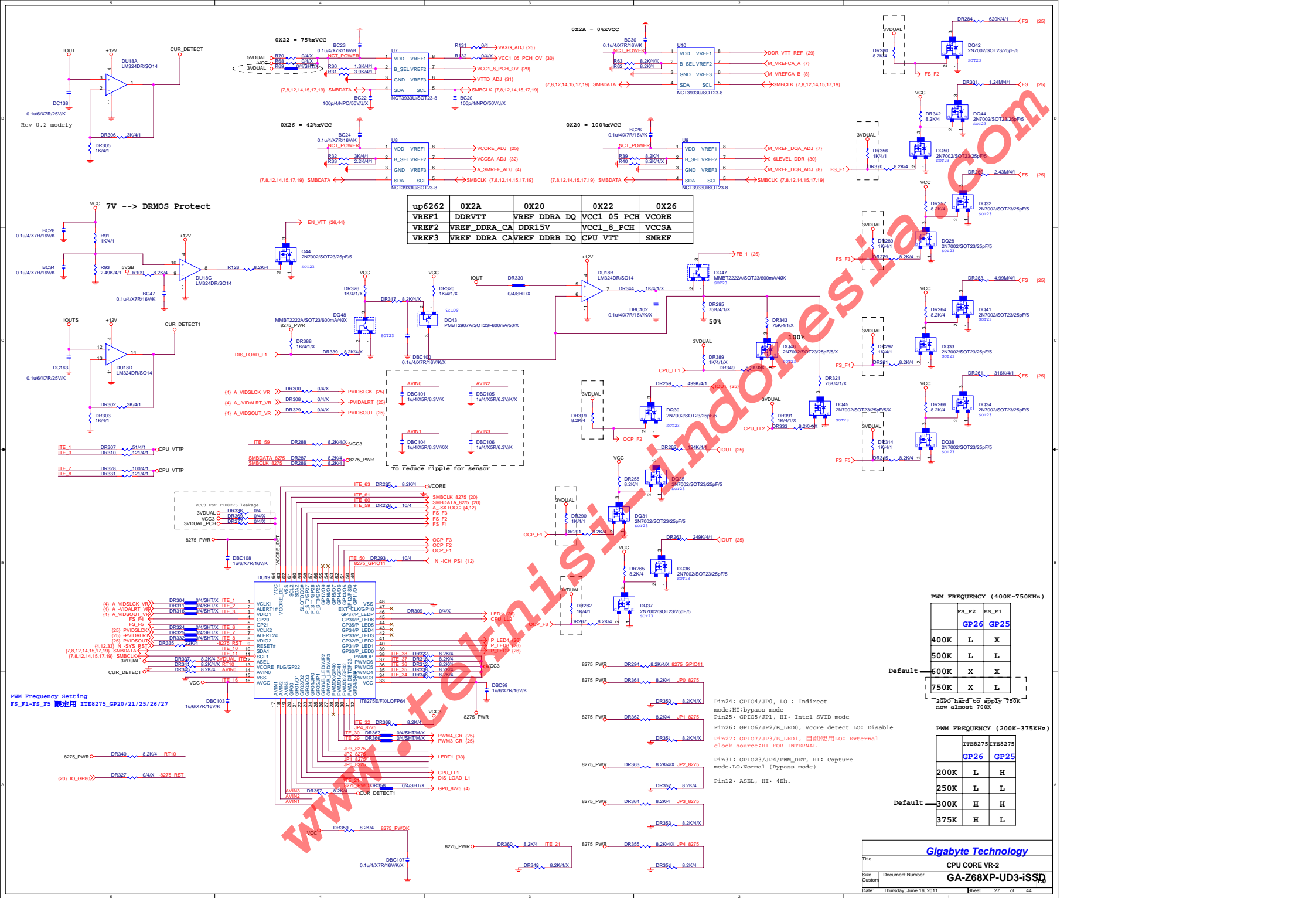


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Title			
AUDIO JACK			
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up6262	0X2A	0X20	0X22	0X26
VREF1	DDRVT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	VCCSA
VREF3	VREF_DDRA_CAVREF_DDRB_DQ		CPU_VTT	SMREF

PWM FREQQUENCY (400K-750KHz)		
	FS_F2	FS_F1
Default	GP26	GP25
400K	L	X
500K	L	L
600K	X	X
750K	X	L

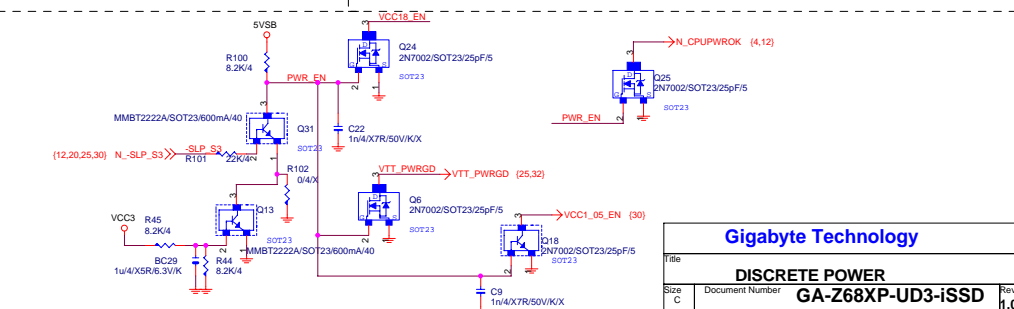
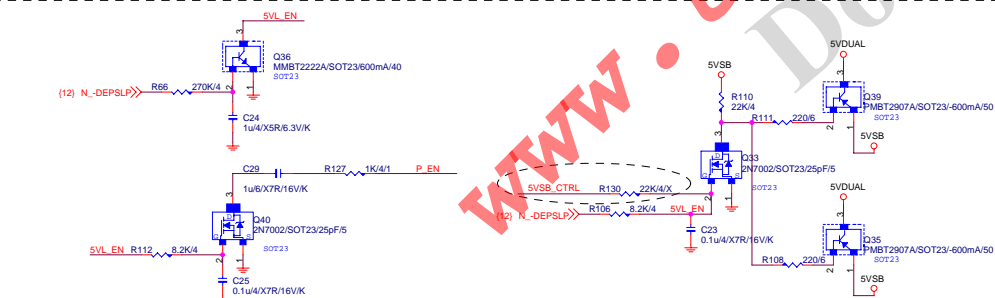
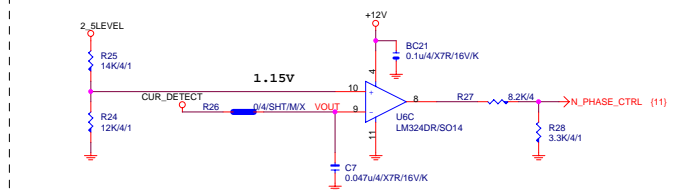
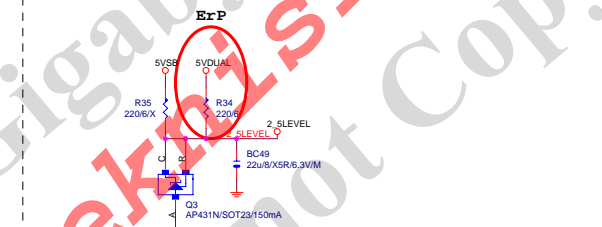
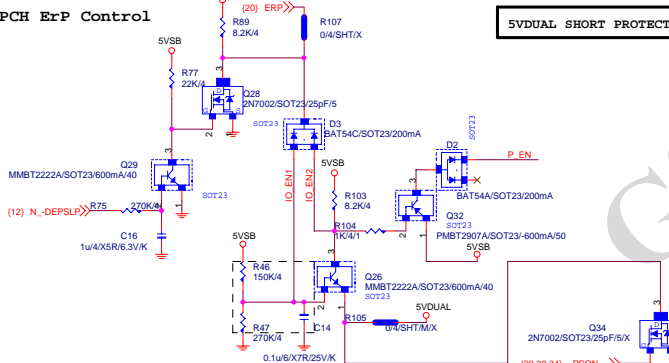
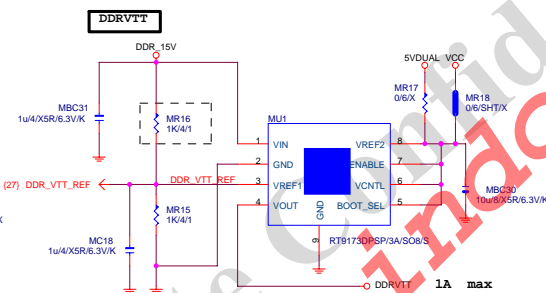
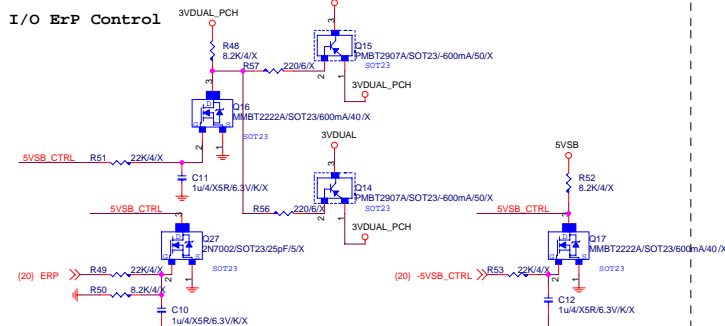
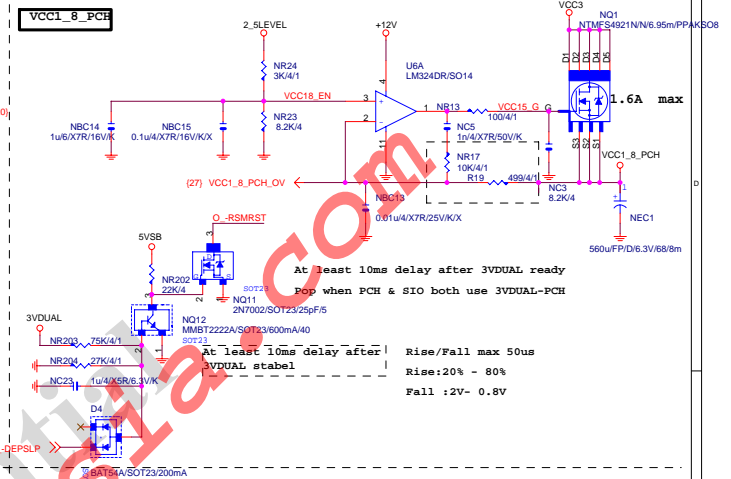
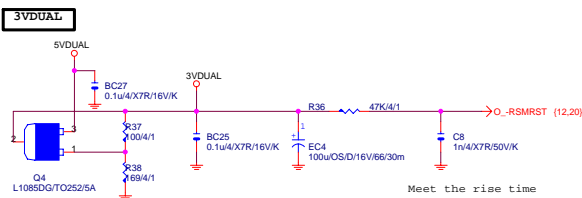
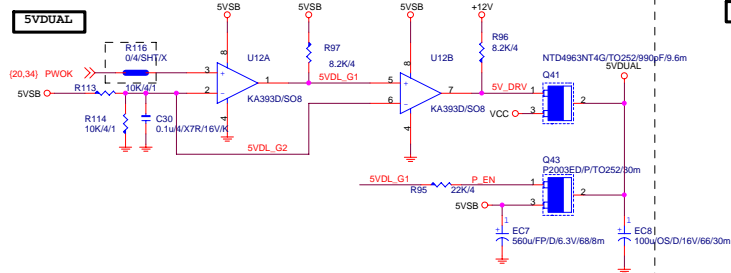
PWM FREQQUENCY (200K-375KHz)		
	ITE8275	ITE8275
Default	GP26	GP25
200K	L	H
250K	L	L
300K	H	H
375K	H	L

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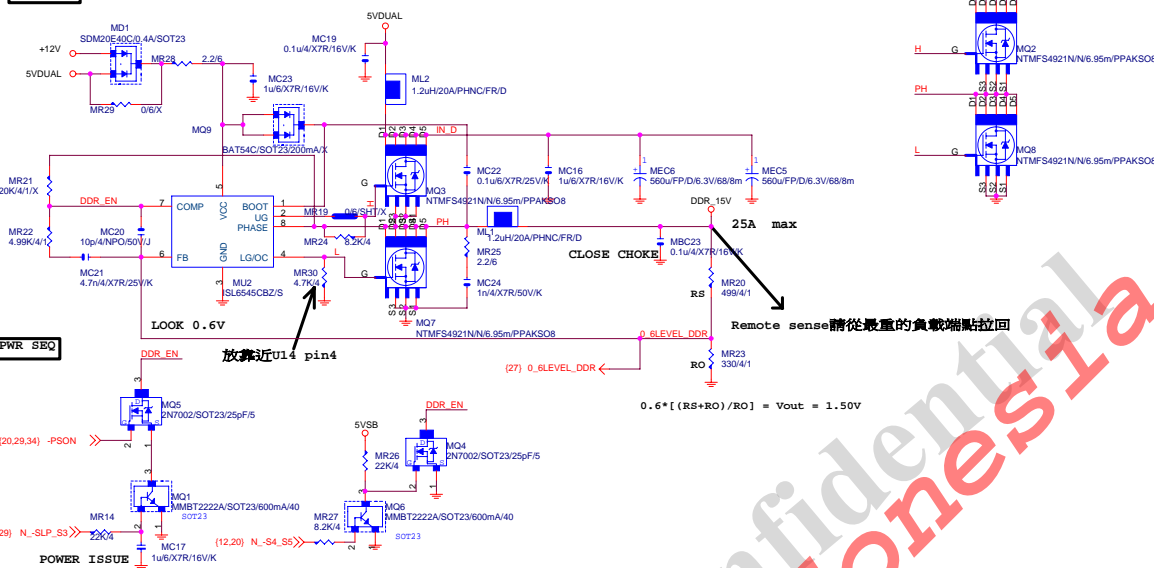
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GIGABYTE™		
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DDR18V

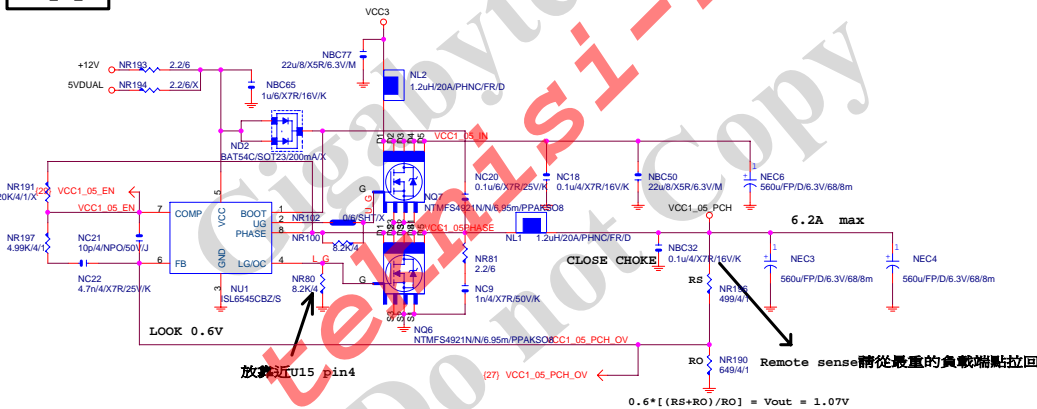


VCC1_05_PCH

OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
 $I_{ocset} = 21.5\mu A$, $R_{ocset} = 8.2k$

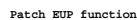
OCP : $I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$
 $= (2 \times 21.5\mu A \times 8.2k) / 7m$
 $= 50.37A$

注意 : R_{ocset} 的阻值要依據 Lo side R_{dson} 改變
 一般 I_{peak} 設定在 50~60A 即可



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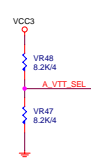
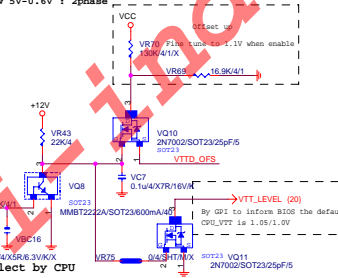
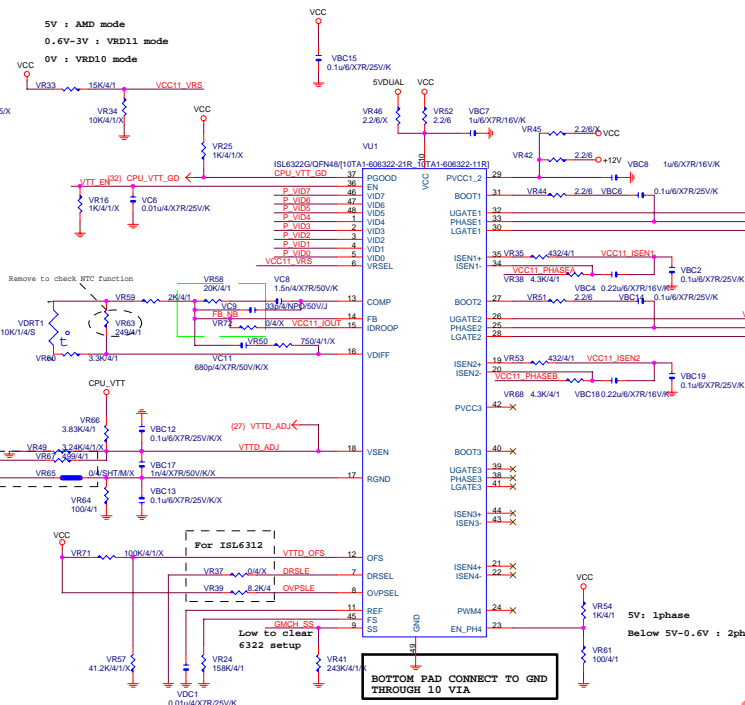
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VCC
VR40 243K/4/1 GMCH_SS
Pu for 6322 type2 SMBus address
address 1000_111x



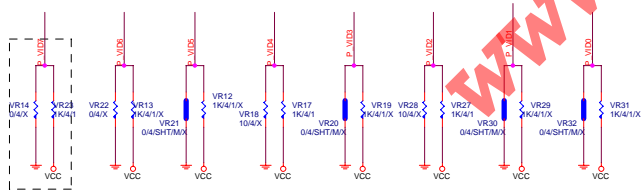
```
5V : AMD mode
0.6V~3V : VRD11 mode
0V : VRD10 mode
```



```

Bit 7 Pull High      Reomve Bit6      AMD 6bit mode
for AMD 6bit          when use AMD      SET 1.05V
mode                  mode              [1x010100]

```



(31) CPU_VTT_GD

VOC3
R54 8.2K/4
VOC3
R99 22K/4
Q10 MMBT2222A/SOT23 600mA/40
C13 0.1μ/4X7R/16V/K/X
VSA REF

(4) A_VSA_SENSE

VOC3
R64 8.2K/4/X
R60 1K/4/1
R58 100K/4/1
Q10 MMBT2222A/SOT23 600mA/40
C18 0.1μ/4X7R/16V/K/X
Q23 2N7002/SOT23/25pF/5
R84 80.6K/4/1
VSA REF

	VSA_SEL
HI	0.85V
LO	0.925V

(27) VCCSA_ADJ

2_5LEVEL
R23 10K/4/1
BC19 0.1μ/4X7R/16V/K
R22 5.23K/4/1
R21 1K/4/1
BC18 0.1μ/4X7R/25V/K/X
R20 0/4/SHT/X
VR74 8.2K/4
Q1 MMBT2222A/SOT23 600mA/40
C12 0.1μ/4X7R/16V/K
CPU_VTT
VR74 8.2K/4
Q1 MMBT2222A/SOT23 600mA/40
C12 0.1μ/4X7R/16V/K
VCCSA
VR62 1K/4/1
VC12 0.1μ/4X7R/16V/K

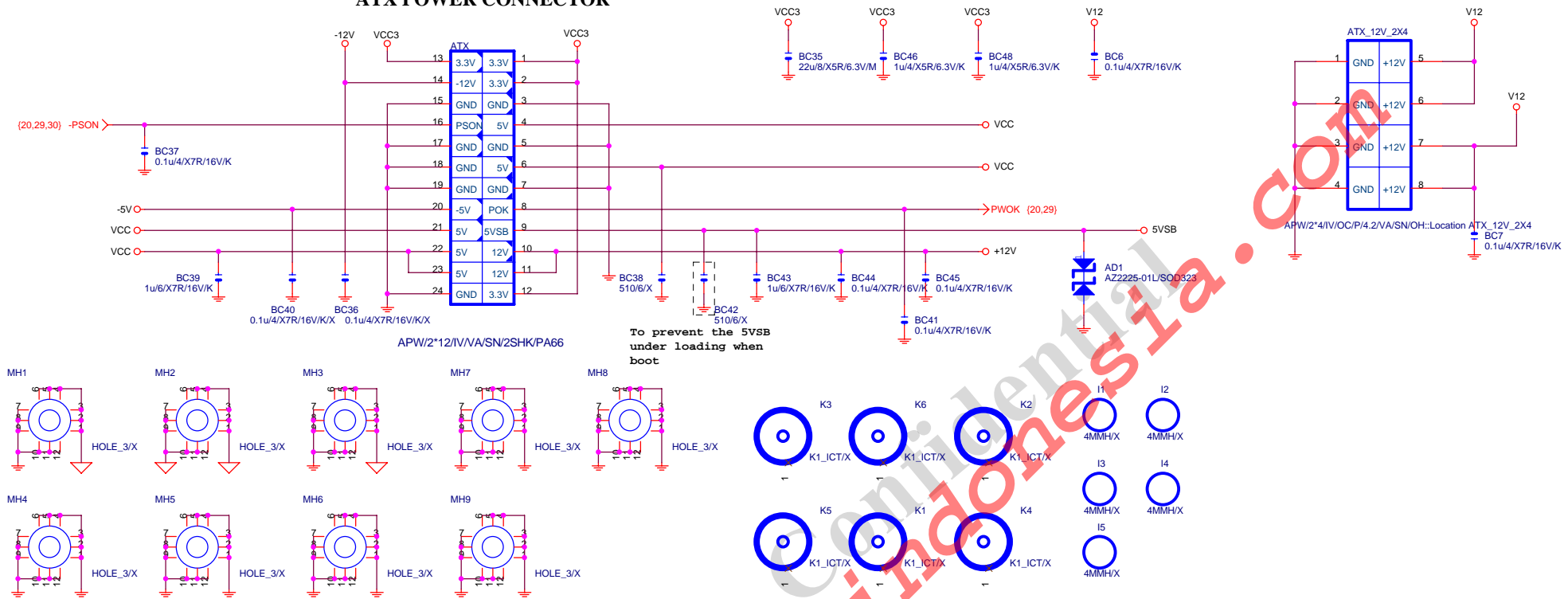
8.8A@0.85V

VCCSA_LEVEL (20)

By GP1 to inform B108 the default VCCSA is 0.925V/0.85V

	VSA_SEL
HI	0.85V
LO	0.925V

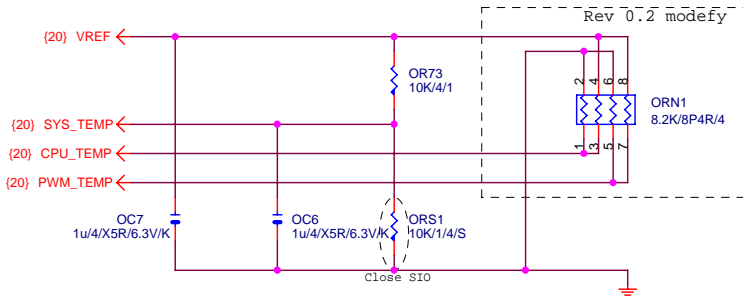
ATX POWER CONNECTOR



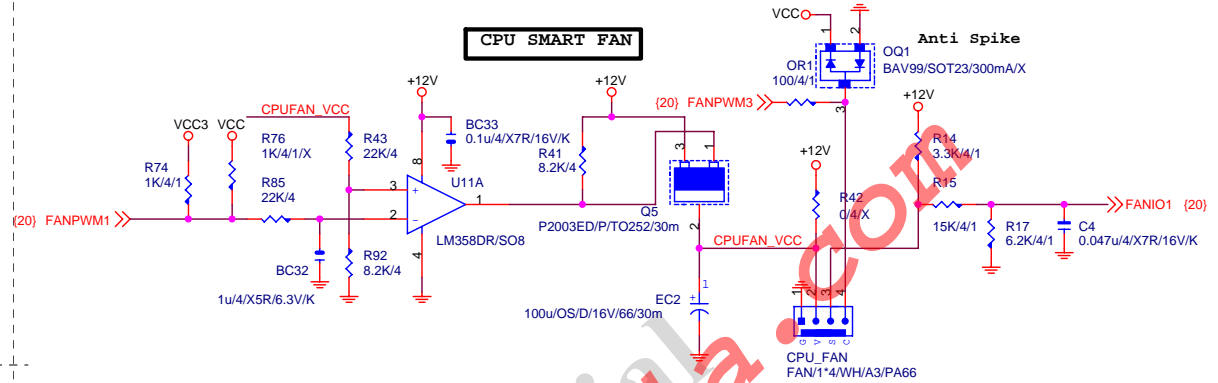
Gigabyte Technology

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Size	Document Number	GA-Z68XP-UD3-iSSD	Rev 1.0
Date:	Thursday, June 16, 2011	Sheet 34	of 44

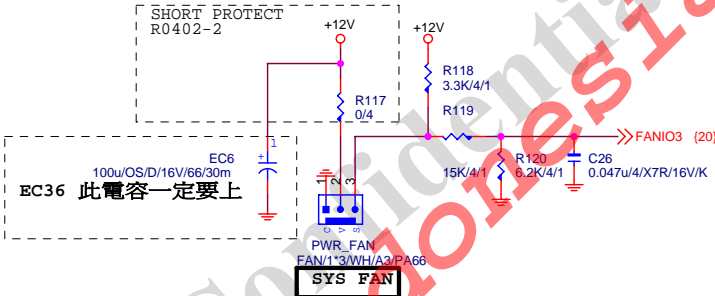
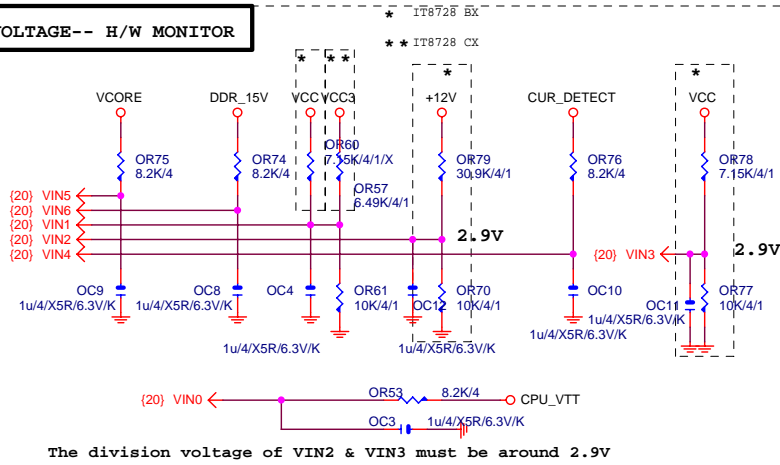
TEMP H/W MONITOR



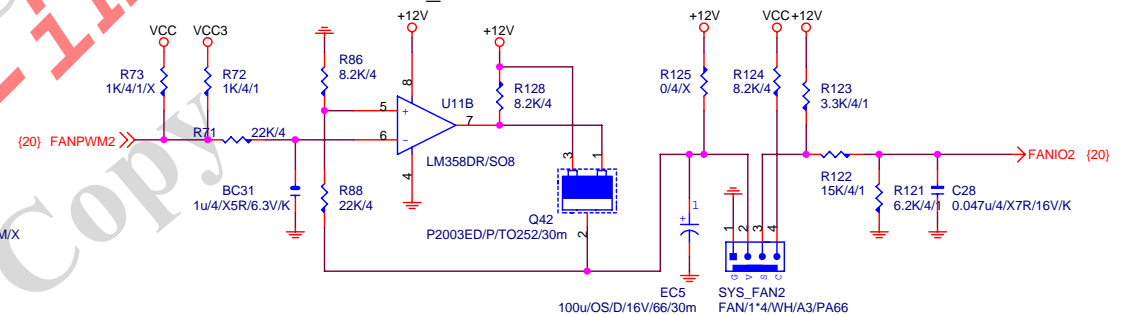
CPU SMART FAN



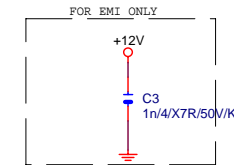
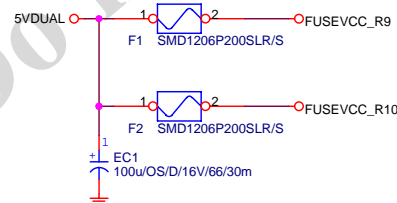
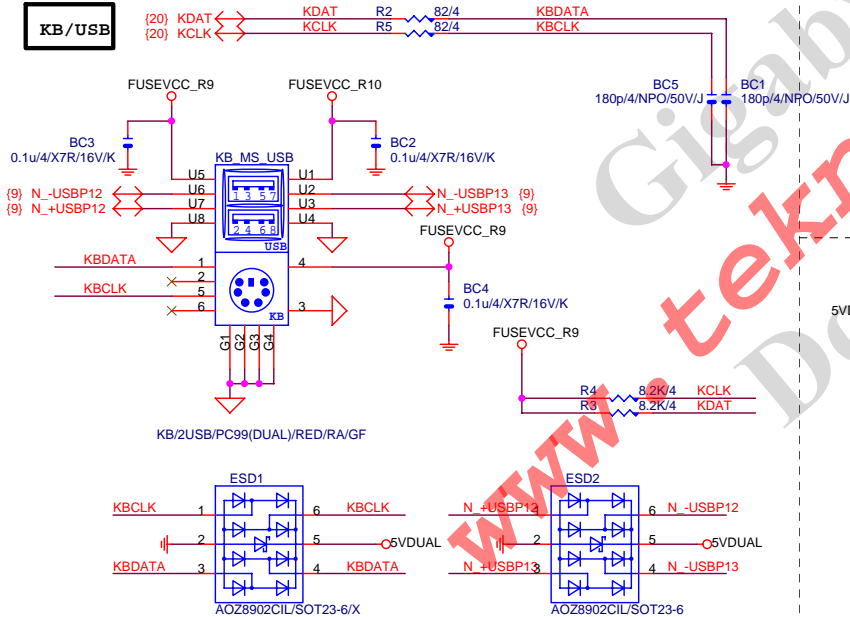
VOLTAGE-- H/W MONITOR



Linear SYS_FAN



KB/USB

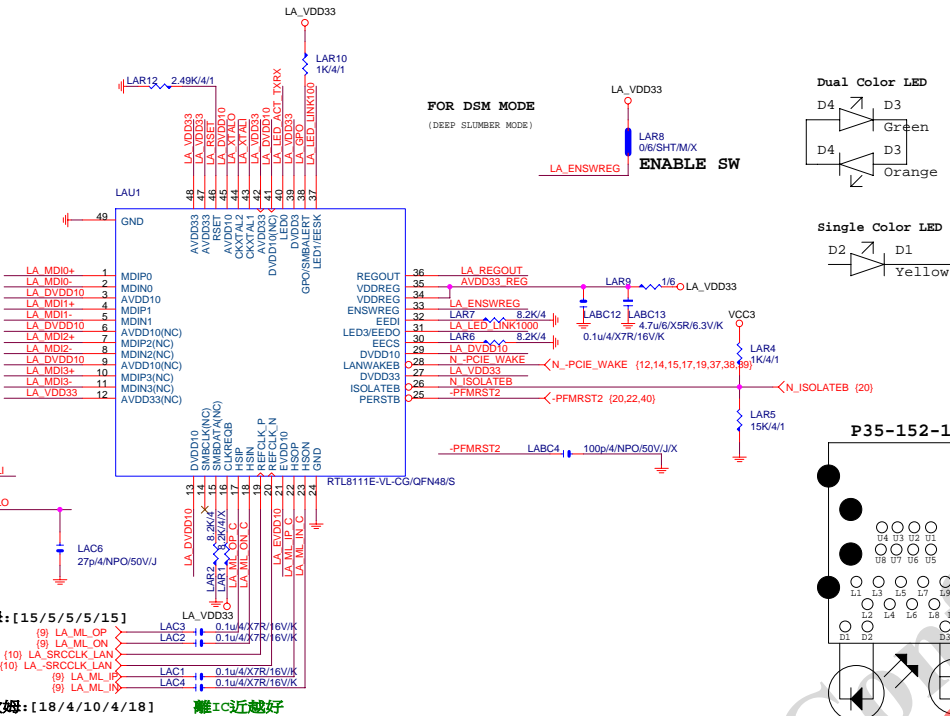


Gigabyte Technology

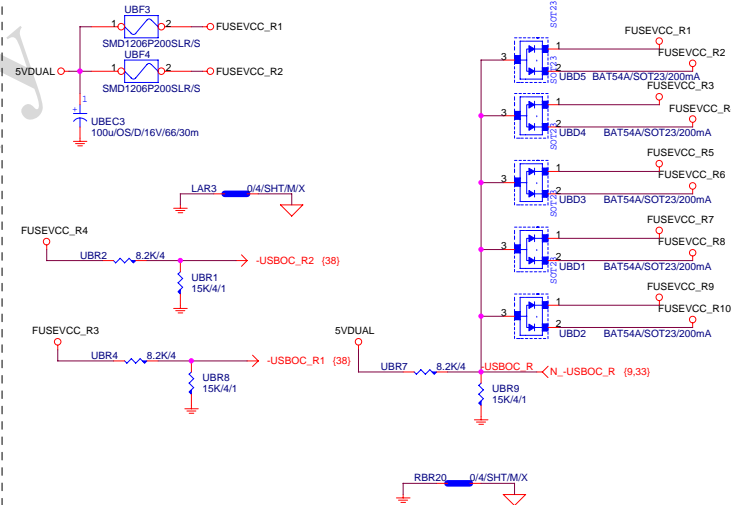
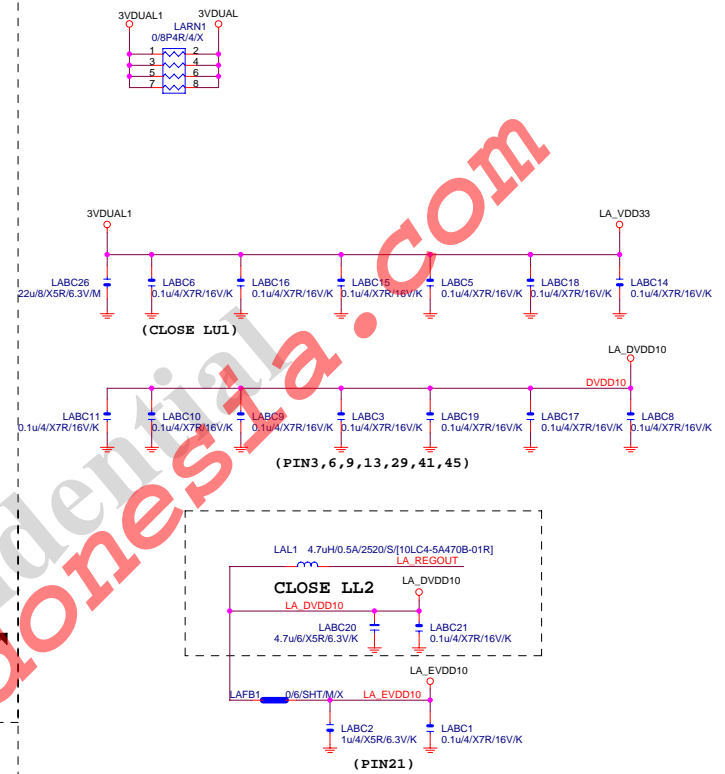
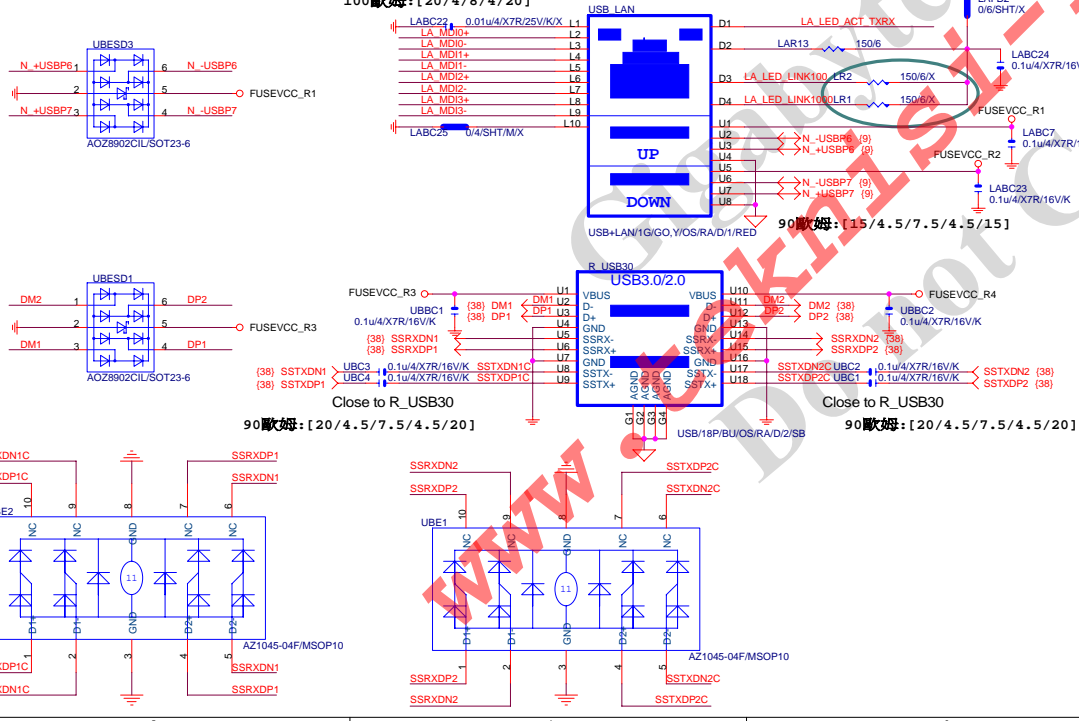
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HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
Custom	GA-Z68XP-UD3-iSSD	1.0	
Date:	Thursday, June 16, 2011	Sheet	35 of 44

Power domain chart

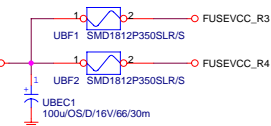
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

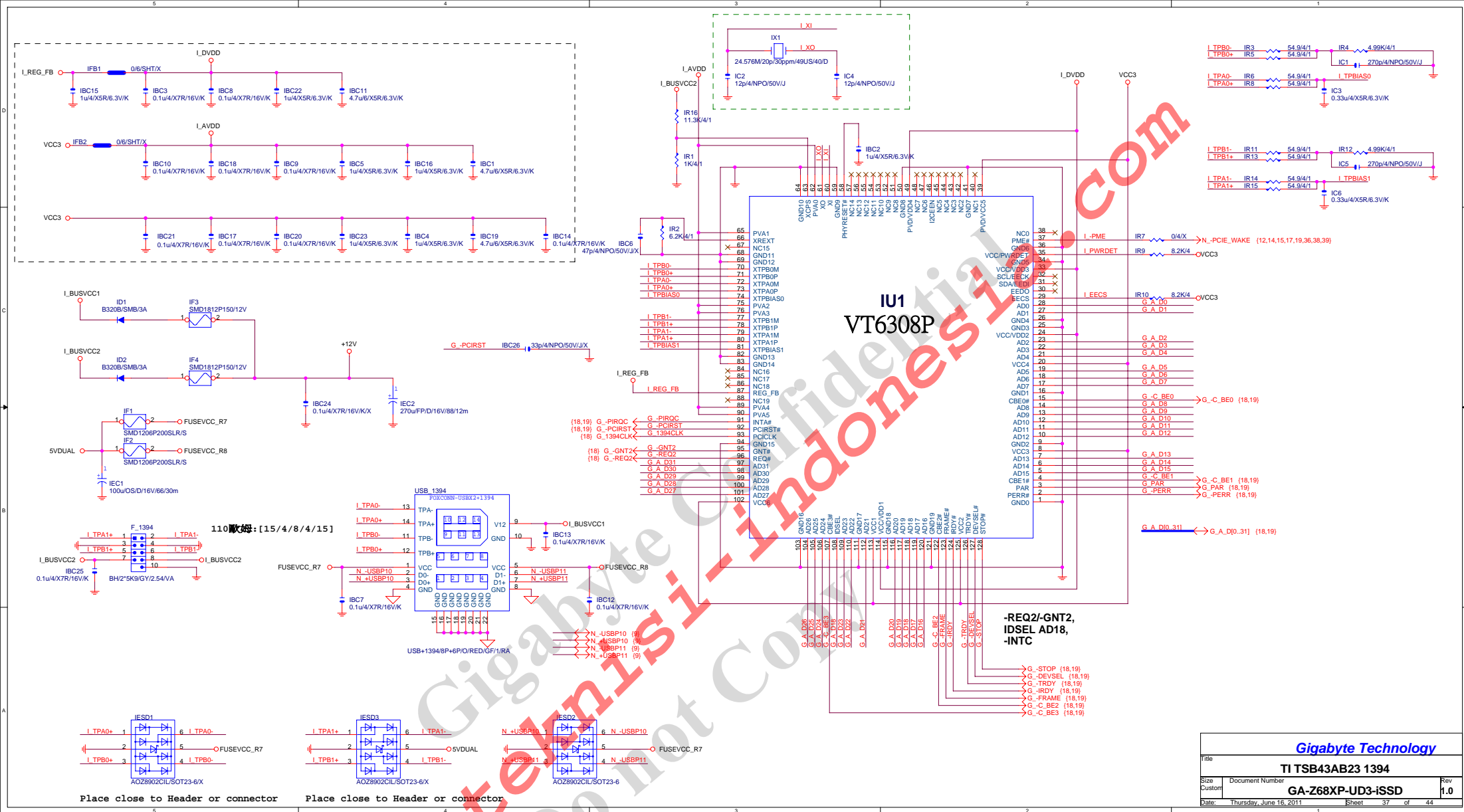


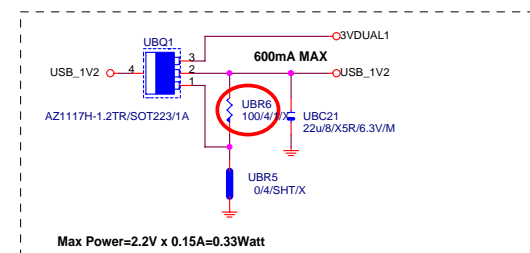
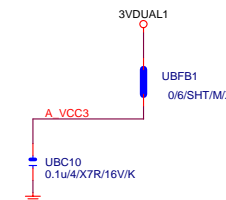
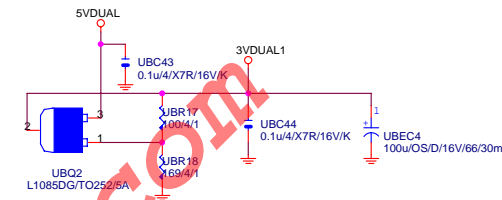
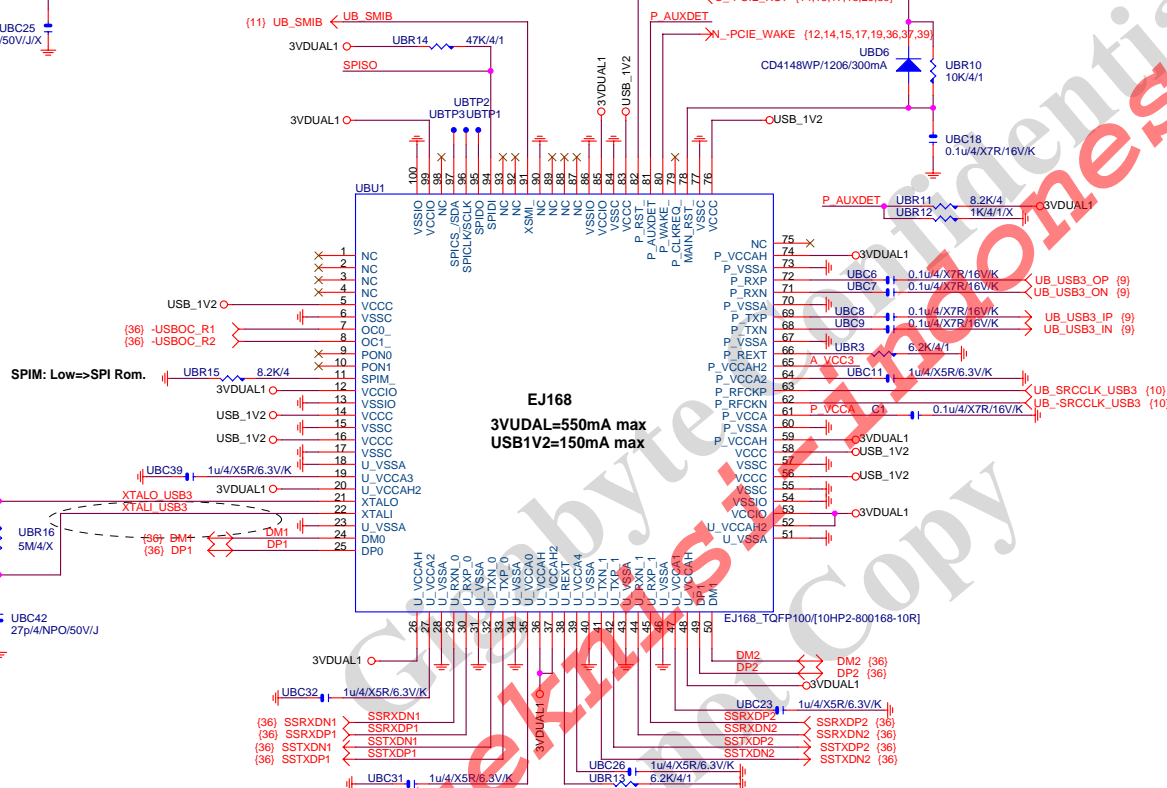
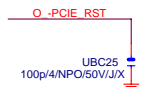
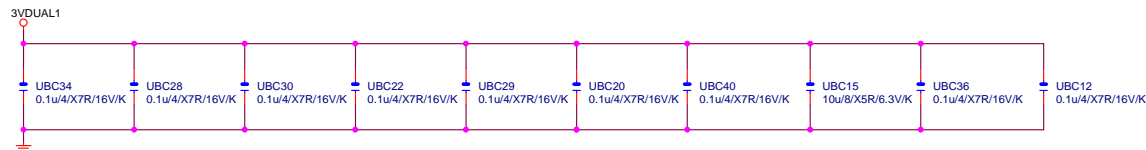
100歐姆:[20/4/8/4/20]



Close to connector



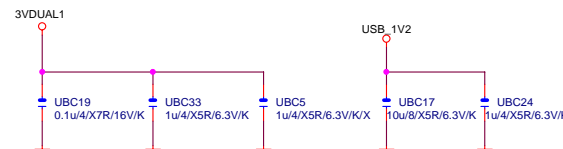
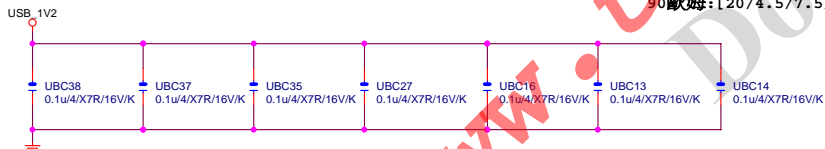




Max Power=2.2V x 0.15A=0.33Watt

AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

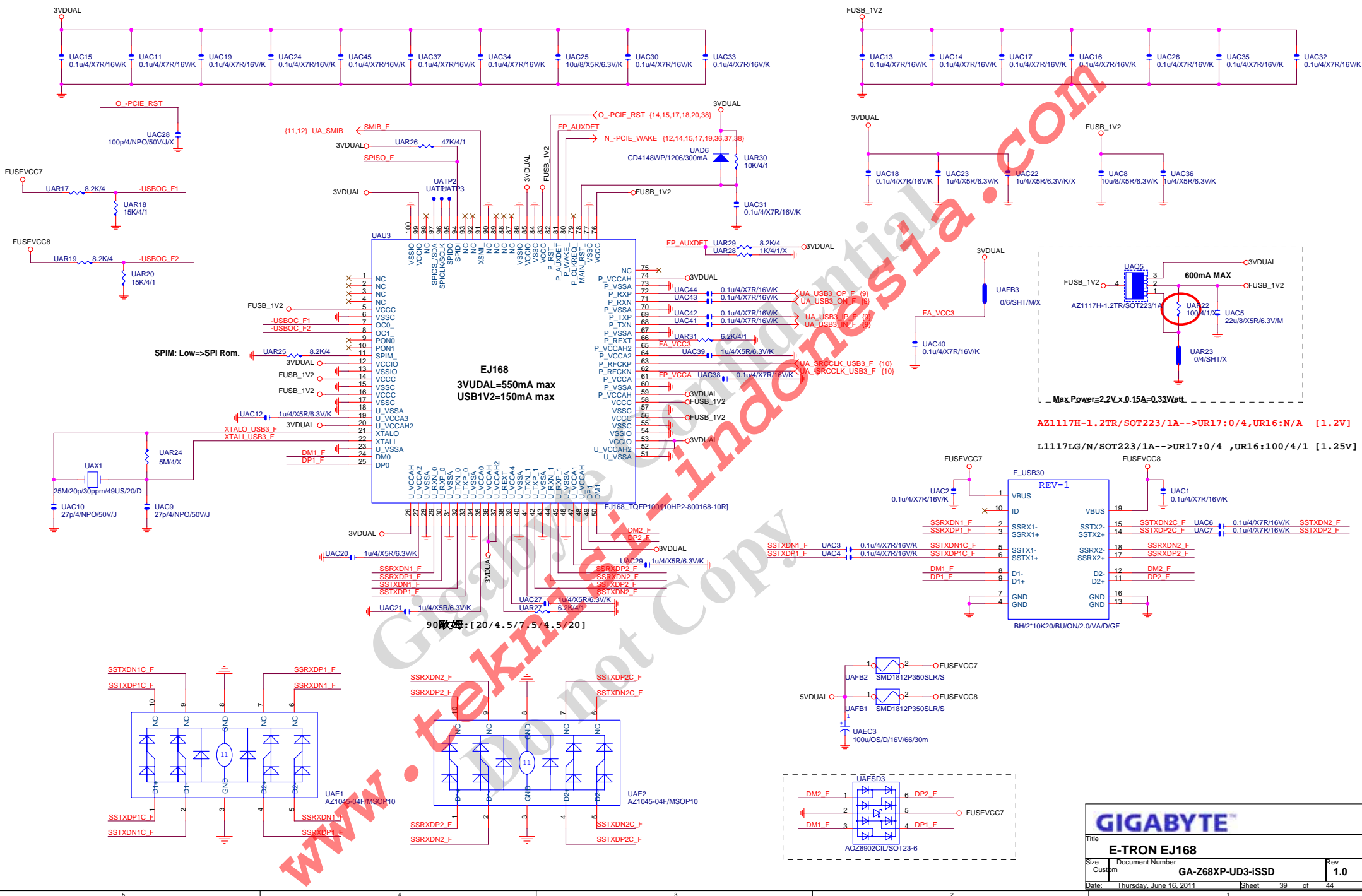
L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]

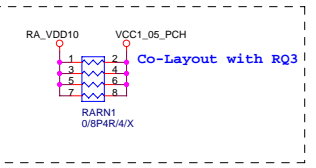
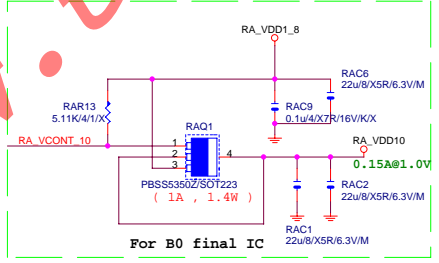
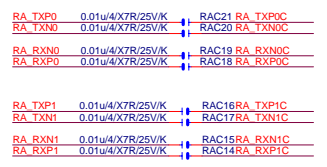
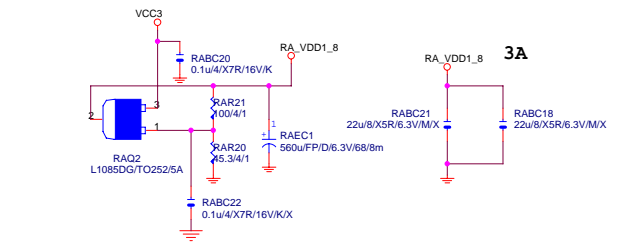
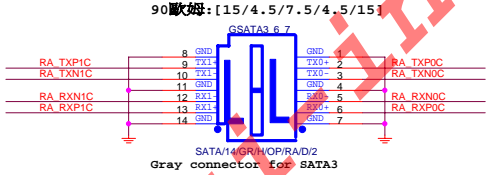
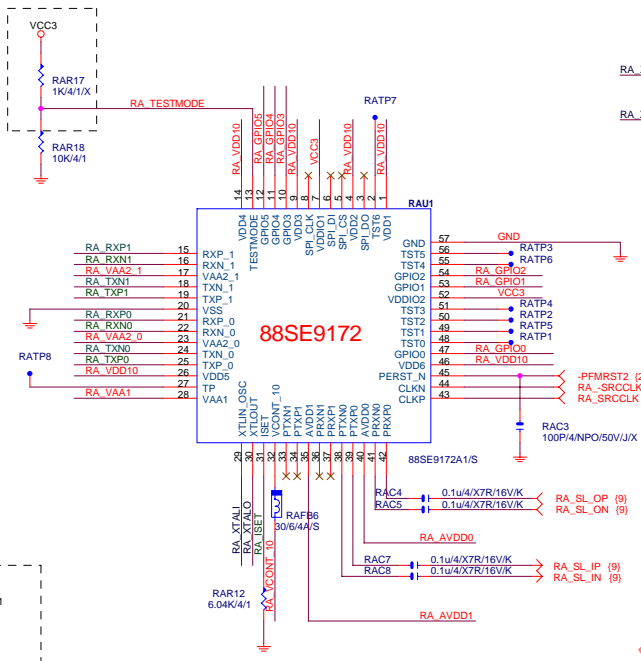
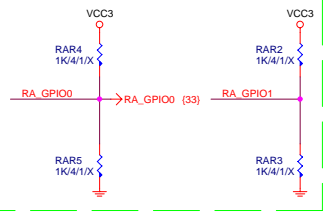
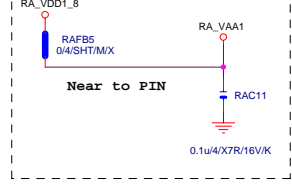
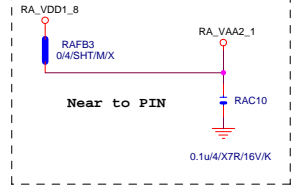
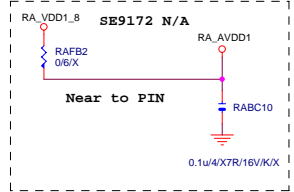
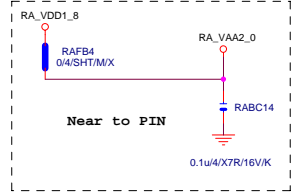
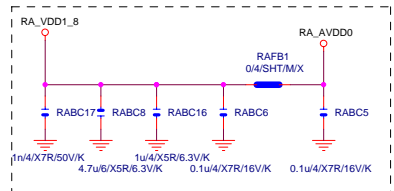
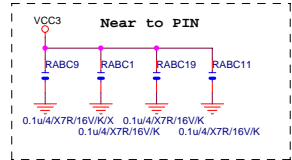
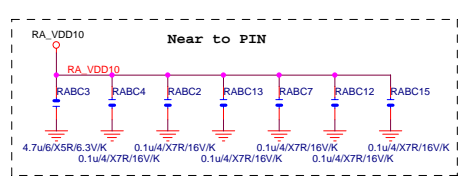


USB3.0 --> 5GHz

BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s

GIGABYTE		
Title		
E-TRON EJ168		
Size	Document Number	Rev
Custom	GA-Z68XP-UD3-ISSD	1.0
Date:	Thursday, June 16, 2011	Sheet 38 of 44





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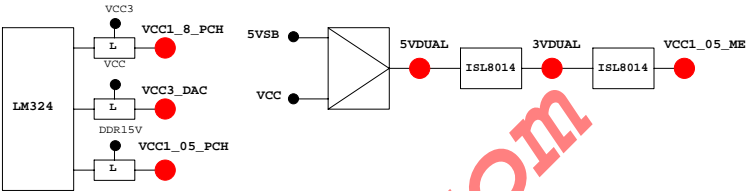
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File		Marvell 9172	
Size	Document Number	GA-Z68XP-UD3-iSSD	
Custom			Rev 1.0
Date:	Thursday, June 16, 2011	Sheet 41	of 44

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQ#	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQ#	P/U 8.2K VCC3	
GP4/PIRQ#	MAIN		GPI -PIRQ#	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_PCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	

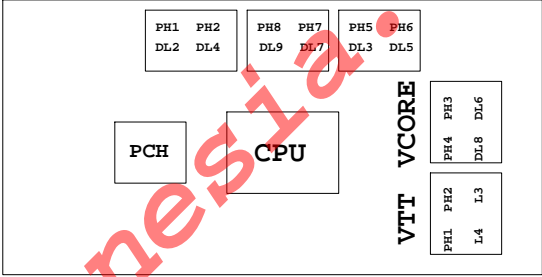
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AED#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMB_D	SRC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

